# S1D13743

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## S1D13743 WQVGA LCD Controller

The S1D13743 is a WQVGA color LCD controller with an embedded 464 KB display buffer. The S1D13743 supports a 8/16-bit Intel 80 CPU architecture while providing high performance bandwidth into display memory allowing for fast screen updates.
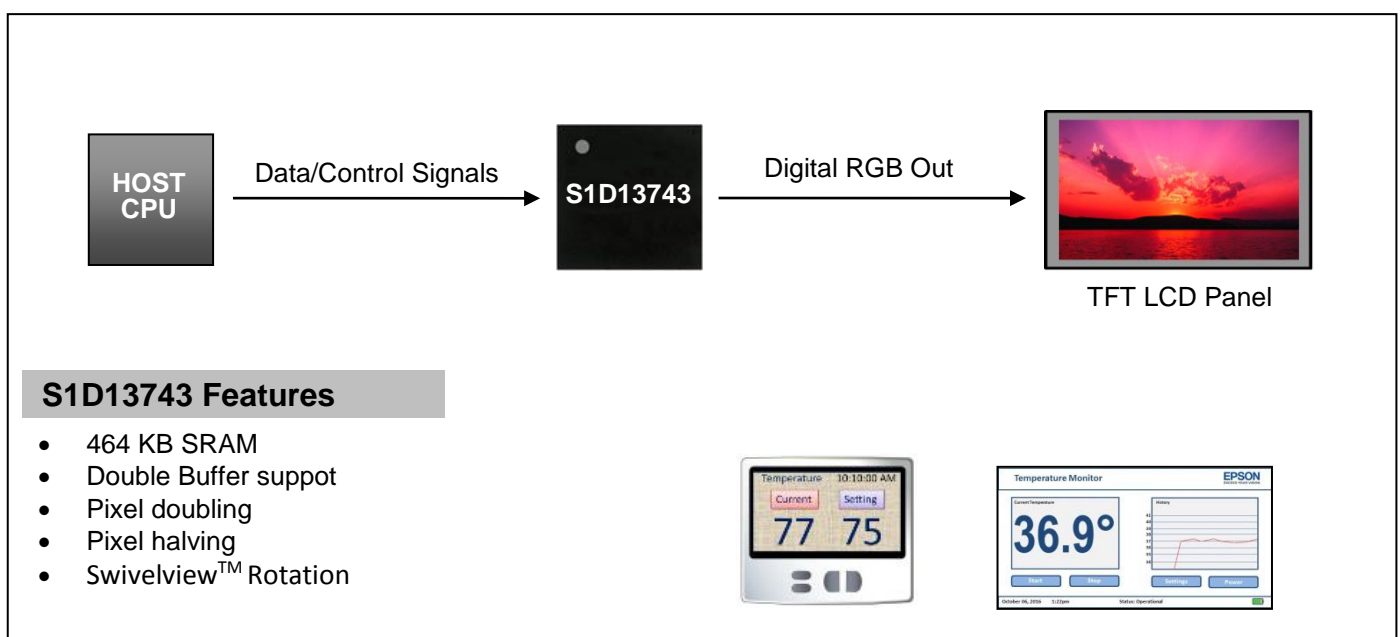
Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. Resolutions supported include 480x272@24bpp single buffered or 320x240@24bpp double-buffered. The S1D13743 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates.

The S1D13743 provides a low cost, low power solution for embedded markets which makes it an ideal display solution for a wide variety of applications.

## FEATURES

- Embedded 464 KB SRAM display buffer
- Low operating voltage
- 8/16-bit Intel 80 interface (used for display or register data)
- Input data formats: RGB 8:8:8, 6:6:6, 5:6:5 and YUV 4:2:2, 4:2:0
- All input data is converted and stored as RGB 8:8:8
- Supports TFT panels
- RGB interface: 18/24-bit
- Supports resolutions up to 352x440
- Hardware / software power save mode
- 24 bpp color depths

- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Double-buffer available to prevent image tearing during streaming input
- Pixel doubling: horizontal and vertical averaging for smooth doubling of a single window
- Pixel halving: no limitation on number of windows
- Internal programmable PLL
- Single MHz clock input: CLKI
- General purpose input/output pins

## SYSTEM BLOCK DIAGRAM



TFT LCD Panel

### S1D13743 Features

- 464 KB SRAM
- Double Buffer suppot
- Pixel doubling
- Pixel halving
- Swivelview™ Rotation

## DESCRIPTION

### Display Buffer

- Embedded 464 KB SRAM display buffer

### CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data)
- Indirect addressing

### Input Data Format

- RGB: 8:8:8, 6:6:6, 5:6:5
- YUV 4:2:2, 4:2:0
- All input data is converted and stored as RGB 8:8:8

### Miscellaneous

- Internal programmable PLL
- Single MHz clock input: CLKI
- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output)
- Hardware/software power save mode
- Input pin to enable/disable power save mode
- General purpose input/output pins are available (GPIO[7:0])
- COREVDD 1.5 volts
  IOVDD 1.65 ~ 3.6 volts
- QFP20 144-pin package

### Display Support

- Supports TFT panels
  - 18/24 bit RGB interface
- Supports resolutions up to 352x440
- Frame rate modulation using 24 bpp data when configured for an 18-bit LCD panel

### Display Features

- 24 bpp color depth
- All display writes are handled by window apertures/position (for complete or partial display updates). All window coordinates are referenced to top left corner of the displayed image (even in a rotated display, the top-left corner is maintained and no host side translation need take place).
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image. All displayed windows can have independent rotation. No additional programming necessary when enabling these modes.
- Double-buffer available to prevent image tearing during streaming input. Resolutions supported must fit inside 384 KB. Typical resolution of 320x240.
- Pixel doubling: horizontal and vertical averaging for smooth doubling of a single window
- Pixel halving: no limitation on number of windows

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For more information on the S1D13743 and other Epson Display Controllers, visit the Epson Global website.

**https://global.epson.com/products_and_drivers/semicon/products/display_controllers/**

For Sales and Technical Support, contact the Epson representative for your region.

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NOTICE: