

## Unity Power Factor LED Lamp Driver

### Features

- Constant Output Current LED Driver
- Large Step-Down Ratio
- Unity Power Factor
- Low-Input Current Harmonic Distortion
- Fixed-Frequency or Fixed Off-Time Operation
- Internal 450V Linear Regulator
- Input and Output Current Sensing
- Input Current Limit
- Enable Pulse-Width Modulation (PWM) Dimming and Phase Dimming

### Applications

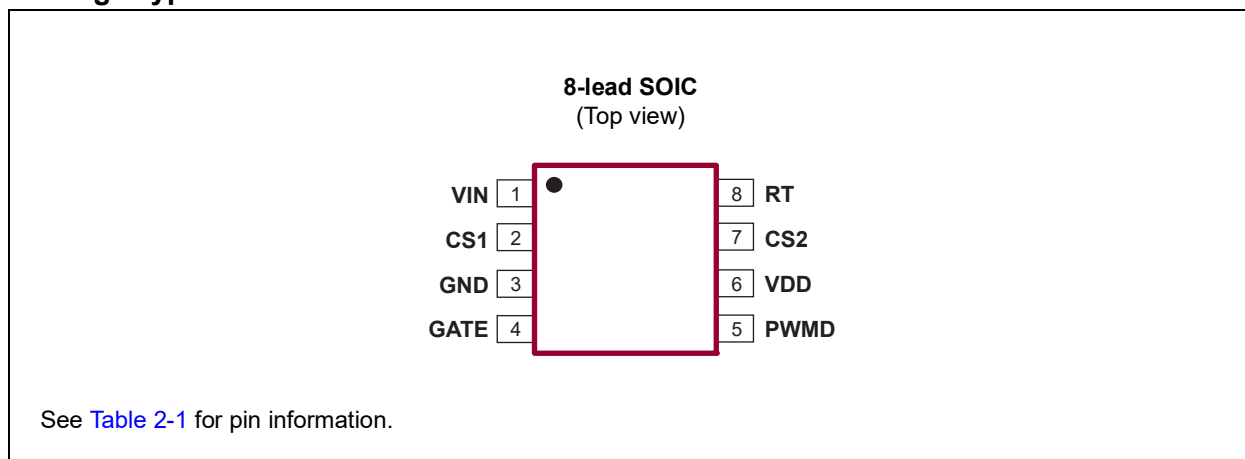
- Offline LED Lamps and Fixtures
- Street Lamps
- Traffic Signals
- Decorative Lighting

### General Description

The HV9931 is a fixed-frequency PWM controller IC designed to control an LED lamp driver using a single-stage PFC buck-boost-buck topology. It can achieve a unity power factor and a very high step-down ratio that enables driving a single high-brightness LED from 85 VAC to 264 VAC input without a power transformer. This topology allows reducing the filter capacitors and using non-electrolytic capacitors to improve reliability. The HV9931 uses open-loop peak current control to regulate both input and output currents. This control technique eliminates the need for loop compensation, limits the input inrush current, and is inherently protected from Input Undervoltage condition.

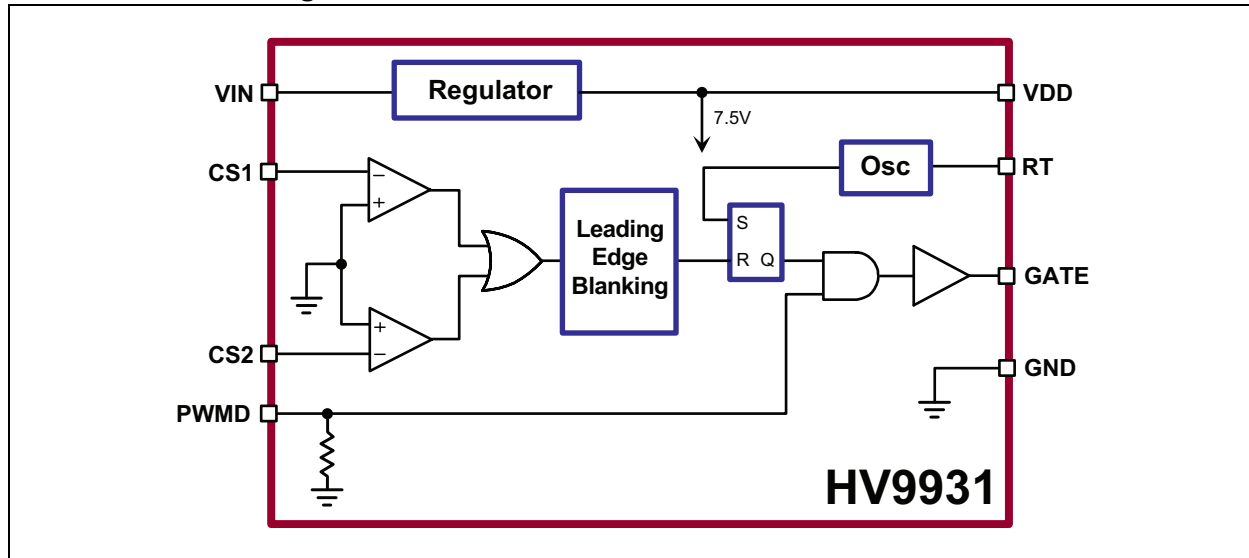
Capacitive isolation protects the LED Lamp from failure of the switching MOSFET. The HV9931 provides a low-frequency PWM dimming input that accepts an external control signal with a duty ratio of 0% to 100% and a frequency of up to a few kilohertz. The PWM dimming capability enables HV9931 phase control solutions that can work with standard wall dimmers.

### Package Type



# HV9931

## Functional Block Diagram





# HV9931

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

|   |                          |
|---|--------------------------|
| $V_{IN}$ to GND .....                                       | -0.5V to +470V           |
| $V_{DD}$ to GND.....  | -0.3V to +13.5V          |
| CS1, CS2, PWMD, GATE, RT to GND.....                        | -0.3V to $V_{DD}$ + 0.3V |
| Junction Temperature, $T_J$ .....                           | -40°C to +150°C          |
| Storage Temperature, $T_S$ .....                            | -65°C to +150°C          |
| Continuous Power Dissipation ( $T_A = +25^\circ\text{C}$ ): |                          |
| 8-lead SOIC .....   | 650 mW                   |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

| Electrical Specifications: Specifications are at $T_A = 25^\circ\text{C}$ . $V_{IN} = 12\text{V}$ unless otherwise noted. |                      |              |      |          |            |  |
|---|----------------------|--------------|------|----------|------------|--|
| Parameter   | Sym.                 | Min.         | Typ. | Max.     | Unit       | Conditions   |
| <b>INPUT</b>  |                      |              |      |          |            |  |
| Input DC Supply Voltage Range   | $V_{INDC}$           | 8            | —    | 450      | V          | DC input voltage ( <b>Note 1</b> )   |
| Shutdown Mode Supply Current  | $I_{INSD}$           | —            | 0.5  | 1        | mA         | PWMD connected to GND ( <b>Note 1</b> )  |
| <b>INTERNAL REGULATOR</b>   |                      |              |      |          |            |  |
| Internally Regulated Voltage  | $V_{DD}$             | 7.12         | 7.5  | 7.88     | V          | $V_{IN} = 8\text{V}$ , $I_{DD(EXT)} = 0\text{ mA}$ , $C_{GATE} = 500\text{ pF}$ , $R_T = 226\text{ k}\Omega$                 |
| $V_{DD}$ Line Regulation  | $\Delta V_{DD,line}$ | 0            | —    | 1        | V          | $V_{IN} = 8\text{V to } 450\text{V}$ , $I_{DD(ext)} = 0\text{ mA}$ , $C_{GATE} = 500\text{ pF}$ , $R_T = 226\text{ k}\Omega$ |
| $V_{DD}$ Undervoltage Lockout Upper Threshold   | $V_{UVLOR}$          | 6.45         | 6.7  | 6.95     | V          | $V_{DD}$ rising  |
| $V_{DD}$ Undervoltage Lockout Hysteresis  | $\Delta V_{UVLO}$    | —            | 500  | —        | mV         |  |
| <b>PWM DIMMING</b>  |                      |              |      |          |            |  |
| PWMD Input Low Voltage  | $V_{PWMD(LO)}$       | —            | —    | 0.80     | V          | $V_{IN} = 8\text{V to } 450\text{V}$ ( <b>Note 1</b> )   |
| PWMD Input High Voltage   | $V_{PWMD(HI)}$       | 2            | —    | —        | V          | $V_{IN} = 8\text{V to } 450\text{V}$ ( <b>Note 1</b> )   |
| PWMD Pull-Down Resistance   | $R_{PWMD}$           | 50           | 100  | 150      | k $\Omega$ | $V_{PWMD} = 5\text{V}$   |
| <b>GATE DRIVER</b>  |                      |              |      |          |            |  |
| GATE Output High Voltage  | $V_{GATE(HI)}$       | $V_{DD}-0.3$ | —    | $V_{DD}$ | V          | $I_{GATE} = 10\text{ mA}$ , $V_{DD} = 7.5\text{V}$ , $V_{IN}$ open ( <b>Note 1</b> )   |
| GATE Output Low Voltage   | $V_{GATE(LO)}$       | 0            | —    | 0.3      | V          | $I_{GATE} = -10\text{ mA}$ , $V_{DD} = 7.5\text{V}$ , $V_{IN}$ open ( <b>Note 1</b> )  |
| GATE Output Rise Time   | $T_{RISE}$           | —            | 30   | 50       | ns         | $C_{GATE} = 500\text{ pF}$ , $V_{DD} = 7.5\text{V}$ , $V_{IN} = \text{open}$   |
| GATE Output Fall Time   | $T_{FALL}$           | —            | 30   | 50       | ns         | $C_{GATE} = 500\text{ pF}$ , $V_{DD} = 7.5\text{V}$ , $V_{IN} = \text{open}$   |
| Delay from CS Trip to GATE  | $T_{DELAY}$          | —            | 150  | 300      | ns         | $V_{CS1}, V_{CS2} = -100\text{ mV}$  |
| Blanking Delay  | $T_{BLANK}$          | 150          | 215  | 280      | ns         | $V_{CS1}, V_{CS2} = -100\text{ mV}$  |
| <b>OSCILLATOR</b>   |                      |              |      |          |            |  |
| Oscillator Frequency  | $F_{OSC}$            | 80           | 100  | 120      | kHz        | $R_T = 226\text{ k}\Omega$   |

**Note 1:** Specifications apply over the full operating ambient temperature range of  $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ .

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$  unless otherwise noted.

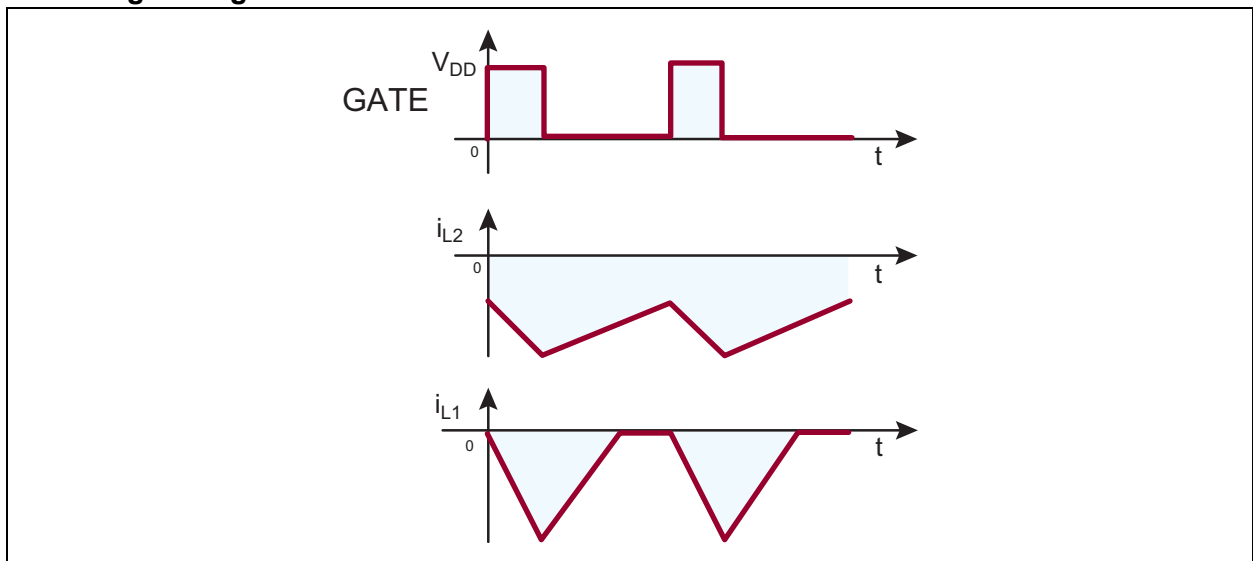
| Parameter   | Sym.                 | Min. | Typ. | Max. | Unit | Conditions |
|---|----------------------|------|------|------|------|------------|
| <b>INPUT AND OUTPUT CURRENT SENSE COMPARATORS</b> |                      |      |      |      |      |            |
| Comparator Input Offset Voltage                   | $V_{\text{OFFSET1}}$ | -15  | —    | 15   | mV   | Note 1     |
|   | $V_{\text{OFFSET2}}$ |      |      |      |      |            |

**Note 1:** Specifications apply over the full operating ambient temperature range of  $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ .

## TEMPERATURE SPECIFICATIONS

| Parameter                         | Sym.                   | Min. | Typ. | Max. | Unit               | Conditions |
|-----------------------------------|------------------------|------|------|------|--------------------|------------|
| <b>TEMPERATURE RANGE</b>          |                        |      |      |      |                    |            |
| Operating Ambient Temperature     | $T_A$                  | -40  | —    | +85  | $^\circ\text{C}$   |            |
| Maximum Junction Temperature      | $T_{\text{J(ABSMAX)}}$ | —    | —    | +150 | $^\circ\text{C}$   |            |
| Storage Temperature               | $T_S$                  | -65  | —    | +150 | $^\circ\text{C}$   |            |
| <b>PACKAGE THERMAL RESISTANCE</b> |                        |      |      |      |                    |            |
| 8-lead SOIC                       | $\theta_{\text{JA}}$   | —    | +101 | —    | $^\circ\text{C/W}$ |            |

## Switching Timing Waveforms



# HV9931

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## 2.0 PIN DESCRIPTION

The details on the pins of HV9931 are listed in [Table 2-1](#). Refer to [Package Type](#) for the location of the pins.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description  |
|------------|----------|--|
| 1          | VIN      | This pin is the input of a high-voltage regulator.   |
| 2          | CS1      | This pin is used to sense the input current of the converter. It is the inverting input of the internal comparator.  |
| 3          | GND      | This is the ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.  |
| 4          | GATE     | This pin is the output of the gate driver for an external N-channel power MOSFET.  |
| 5          | PWMD     | When this pin is pulled to GND, switching of the HV9931 is disabled. When the PWMD pin is released or the external TTL high level is applied to it, switching will resume. This feature is provided for applications that require PWM dimming of the LED lamp. |
| 6          | VDD      | This is a power supply pin for all internal circuits. It must be bypassed with a low-ESR capacitor to GND.   |
| 7          | CS2      | This pin is used to sense the output current of the converter. It is the inverting input of the internal comparator.   |
| 8          | RT       | Oscillator control. A resistor connected between this pin and GND sets the switching frequency. A resistor connected between this pin and the GATE pin sets the switching off-time.  |

## 3.0 DETAILED DESCRIPTION

### 3.1 Power Topology

The HV9931 is optimized to drive Microchip's proprietary single-stage, single-switch, non-isolated topology, cascading an input power factor correction (PFC) buck-boost stage and an output buck converter power stage. (Refer to [Typical Application Circuit.](#)) This power converter topology offers numerous advantages useful for driving high-brightness light-emitting diodes (HB LED). These advantages include unity power factor, low harmonic distortion of the input AC line current, and low output current ripple. The output load is decoupled from the input voltage with a capacitor, making the driver inherently failure-safe for the output load. The power converter topology also permits reducing the size of the filter capacitor needed, enabling the use of non-electrolytic capacitors. This feature greatly improves the reliability of the overall solution.

The HV9931 is a Peak Current-mode controller that is specifically designed to drive a constant-current buck-boost-buck power converter. This patented control scheme features two identical current sense comparators for detecting negative current signal levels. One of the comparators regulates the output LED current, while the other is used for sensing the input inductor current. The second comparator is mainly responsible for the converter start-up. The control scheme inherently features low inrush current and input undervoltage protection. The HV9931 can operate with programmable constant frequency or Constant Off-time Operating mode. In many cases, the Constant Off-time Operating mode is preferred because it improves line regulation of the output current, reduces voltage stress of the power components, and simplifies regulatory EMI compliance. (See application note, *AN-H52 HV9931 Unity Power Factor LED Lamp Driver.*)

### 3.2 Input Voltage Regulator

The HV9931 can be powered directly from its  $V_{IN}$  pin that can take a voltage from 8V to 450V. When voltage is applied to the  $V_{IN}$  pin, the HV9931 attempts at regulating a constant 7.5V (typical) at the  $V_{DD}$  pin. The  $V_{DD}$  voltage can be also used as a voltage reference for the current sense comparators. The regulator is equipped with an undervoltage protection circuit, which shuts off the HV9931 when the voltage at the  $V_{DD}$  pin falls below 6.2V.

The  $V_{DD}$  pin must be bypassed by a low-ESR capacitor ( $\geq 0.1 \mu\text{F}$ ) to provide a low-impedance path for the high-frequency current of the output gate driver.

The HV9931 can also be operated by supplying voltage at the  $V_{DD}$  pin greater than the internally regulated voltage. This will turn off the internal linear regulator, and the HV9931 will function by drawing power from the external voltage source connected to the  $V_{DD}$  pin.

For input transients that reduce the input voltage below 8V (e.g. Cold Crank condition in an automotive system), the  $V_{IN}$  pin of the HV9931 can be connected to the MOSFET drain through a diode. Since the drain of the FET is at a voltage equal to the sum of the input and output voltages, the IC will still be operational when the input goes below 8V. In this case, a larger capacitor is needed for the  $V_{DD}$  pin to supply power to the IC when the MOSFET is switched on.

### 3.3 PWM Dimming and Wall Dimmer Compatibility

PWM Dimming can be achieved by applying a TTL-compatible square wave signal at the PWMD pin. When the PWMD pin is pulled high, the gate driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the gate driver is disabled and the external MOSFET turns off. The HV9931 is designed to make the signal at the PWMD pin inhibit the driver only, and the IC need not go through the entire start-up cycle each time, ensuring a quick response time for the output current.

The power topology requires little filter capacitance at the output since the output current of the buck stage is continuous, and AC line filtering is accomplished through the middle capacitor rather than the output capacitor. Therefore, disabling the HV9931 via its PWMD pin or  $V_{IN}$  pin can interrupt the output LED current in accordance with the phase-controlled voltage waveform of a standard wall dimmer.

### 3.4 Oscillator

Connecting an external resistor from RT pin to GND programs switching frequency. See [Equation 3-1](#).

**EQUATION 3-1:**

$$F_{SW}[kHz] = \frac{25000}{R_T[k\Omega] + 22}$$

On the other hand, connecting the resistor from the RT pin to the GATE pin programs Constant Off-Time. Refer to [Equation 3-2](#).

**EQUATION 3-2:**

$$T_{OFF}[\mu s] = \frac{R_T[k\Omega] + 22}{25}$$

## 3.5 Input and Output Current Sensing

Two current sense comparators are included in the HV9931. Both comparators have their non-inverting inputs internally connected to GND. The CS<sub>1</sub> and CS<sub>2</sub> inputs are inverting inputs of the comparators. Connecting a resistor divider to either of these inputs from a positive reference voltage and a negative current sense voltage signal programs the current sense threshold of the comparator. The V<sub>DD</sub> voltage of the HV9931 can be used as reference voltage. If more accuracy is needed, an external reference voltage can be applied. When either the CS<sub>1</sub> or the CS<sub>2</sub> pin voltage falls below GND, the gate pulse is terminated. A leading edge blanking delay of 215 ns (typical) is added. The gate voltage becomes high again upon receiving the next clock pulse of the oscillator circuit.

Referring to Figure 3-1, the CS2 comparator is responsible for regulating output current. The output LED current can be programmed using Equation 3-3.

### EQUATION 3-3:

$$R_{CS2} = \frac{I_O + \frac{\Delta I_{L2}}{2}}{7.5V} \times R_{REF2} \times R_{S2}$$

Where  $\Delta I_{L2}$  is the peak-to-peak current ripple in L2.  
 $I_O$  is the average output LED current.

The CS1 comparator limits the current in the input inductor L1. There is no charge in the capacitor C1 upon the start-up of the converter. Therefore, L2 cannot develop the output current, and the HV9931 starts up in Input Current Limiting mode. The CS1 current threshold must be programmed such that no input current limiting occurs in normal Steady-state operation. The CS1 threshold can be programmed in accordance with a similar equation. Refer to Equation 3-4.

### EQUATION 3-4:

$$R_{CS1} = \frac{I_{L1(PK)}}{7.5V} \times R_{REF1} \times R_{S1}$$

Where  $I_{L1(PK)}$  is the maximum peak current in L1.

## 3.6 MOSFET Gate Driver

The gate driving capability of the HV9931 is typically limited by the amount of power dissipation in its linear regulator. Thus, care must be taken when selecting a switching MOSFET to be used in the circuit. An optimal trade-off must be found between the gate charge and the MOSFET's on-resistance to minimize the input regulator current.

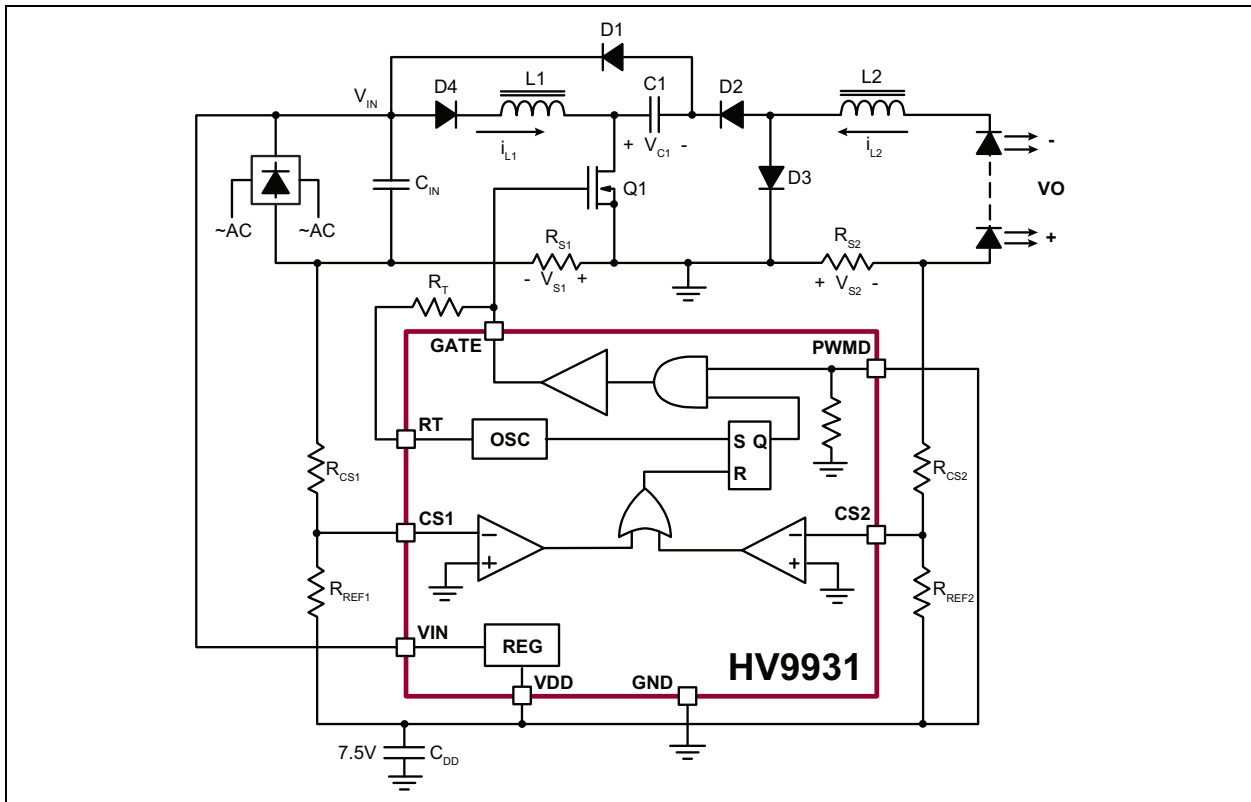


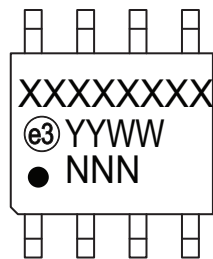
FIGURE 3-1: Functional Circuit Diagram.



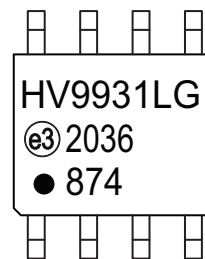
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

8-lead SOIC

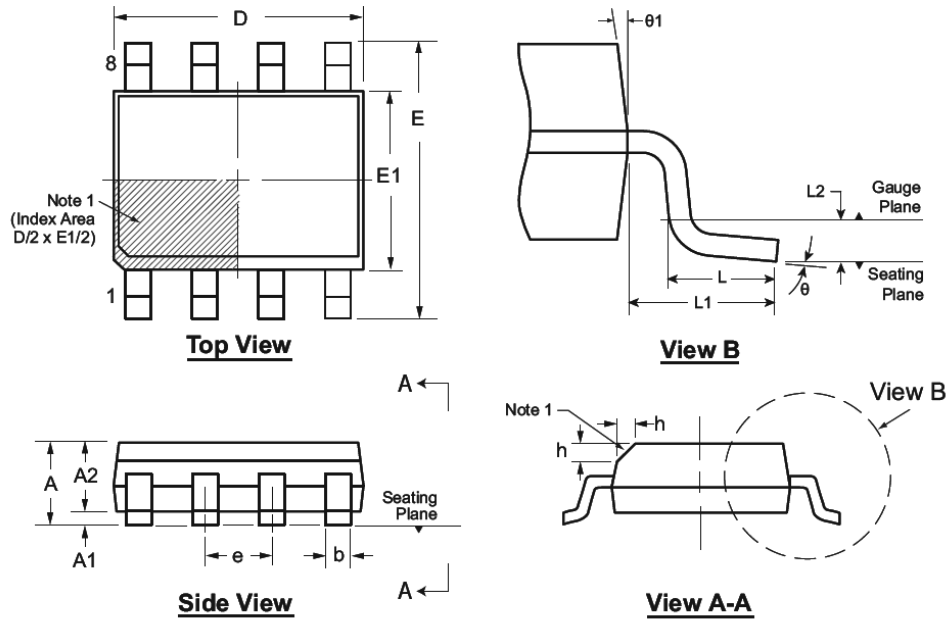


Example



|                |  |  |
|----------------|--|--|
| <b>Legend:</b> | XX...X   | Product Code or Customer-specific information  |
|                | Y  | Year code (last digit of calendar year)  |
|                | YY   | Year code (last 2 digits of calendar year)   |
|                | WW   | Week code (week of January 1 is week '01')   |
|                | NNN  | Alphanumeric traceability code   |
|                | e3   | Pb-free JEDEC® designator for Matte Tin (Sn)   |
|                | *  | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |
| <b>Note:</b>   | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo. |  |

## 8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Note:**

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol         | A   | A1    | A2   | b     | D    | E     | E1    | e     | h           | L    | L1   | L2          | $\theta$    | $\theta_1$ |    |     |
|----------------|-----|-------|------|-------|------|-------|-------|-------|-------------|------|------|-------------|-------------|------------|----|-----|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25  | 0.31 | 4.80* | 5.80* | 3.80* | 1.27<br>BSC | 0.25 | 0.40 | 1.04<br>REF | 0.25<br>BSC | 0°         | 5° |     |
|                | NOM | -     | -    | -     | -    | 4.90  | 6.00  | 3.90  |             | -    | -    |             | -           | -          | -  | -   |
|                | MAX | 1.75  | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* |             | 0.50 | 1.27 |             | -           | -          | 8° | 15° |

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

## APPENDIX A: REVISION HISTORY

### Revision A (May 2020)

- Converted Supertex Doc# DSFP-HV9931 to Microchip DS20005733A
- Changed the part marking format
- Updated the quantity of the 8-lead SOIC LG package from 2500/Reel to 3300/Reel to align it with the actual BQM
- Made minor text changes throughout the document

# HV9931

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | <u>XX</u>       | - | <u>X</u>                              | - | <u>X</u>   |
|-----------------|-----------------|---|---------------------------------------|---|------------|
| Device          | Package Options |   | Environmental                         |   | Media Type |
| Device:         | HV9931          | = | Unity Power Factor LED Lamp Driver    |   |            |
| Package:        | LG              | = | 8-lead SOIC                           |   |            |
| Environmental:  | G               | = | Lead (Pb)-free/RoHS-compliant Package |   |            |
| Media Type:     | (blank)         | = | 3300/Reel for an LG Package           |   |            |

**Example:**

a) HV9931LG-G: Unity Power Factor LED Lamp Driver, 8-lead SOIC Package, 3300/Reel

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