Keywords: E1, T1, unframed, CRC4, ESF, D4, BITS

APPLICATION NOTE 6542

REGISTER CONFIGURATION FOR DS26504

Abstract: This application note describes the basic register settings to configure the DS26504 for operation in various modes. The device supports three modes each for E1 and T1 operation—for E1, the DS26504 supports unframed mode, as well as CRC4 and FAS framing structure modes; for T1, the device supports unframed mode, as well as D4 and ESF framing structure modes. The DS26504 can also be configured to operate with the G.703 and 6312kHz synchronization interfaces, as well as the 64kHz composite clock interface.

Introduction

The DS26504 is a building-integrated timing supply (BITS) clock-recovery element that also functions as a reduced function set single-chip transceiver. The receiver portion of this device can recover a clock from E1 and T1, the G.703 and 6312kHz synchronization interfaces, and the 64kHz composite clock interface. This application note describes how to configure DS26504 registers for operating in each these modes.

Table 1. Acronym Definitions

Acronym	Description
CRC	Cyclic Redundancy Check
ESF	Extended Super Frame
FAS	Frame Alignment Signal
SF	Superframe

Operating Modes

Configuring the MCREG register allows the user to set the DS26504 to operate in the following modes:

- E1 Modes
  - Unframed
  - CRC4 Framing Structure
  - FAS Framing Structure
- T1 Modes
  - Unframed
  - D4 Framing Structure
  - ESF Framing Structure
- G.703 2.048MHz Synchronous Interface Mode
- 6312kHz Synchronization Interface Mode
- 64kHz Composite Clock Mode

E1 Mode

The DS26504 supports unframed and framed E1 modes. This section provides detailed register settings for E1 unframed mode as well as those for the CRC4 and FAS framing structures.

Table 2. Register Settings for E1 Mode—Unframed

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0x66
0x8009	TPCR1	0x48
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x40
0x801D	E1RCR	0x20
0x801E	E1TCR	0x02
0x8001	IOCR1	0x80
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x00
0x8012	INFO2	0x00
0x801C	INFO3	0x00
0x8013	IIR	0x00
0x8014	SR1	0x12
0x8015	IMR1	0x00
0x8016	SR2	0x3A
0x8017	IMR2	0x00
0x8018	SR3	0x00

0x8019	IMR3	0x00
0x801A	SR4	0x3F
0x801B	IMR4	0x00
0x8021	SR5	0x1F
0x8022	IMR5	0x00
0x8030	LIC1	0x11
0x8031	LIC2	0x08
0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0x9B
0x8057	RNAF	0xC0
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x4B
0x8059	RSiNAF	0x2F
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

Table 3. Register Settings for E1 Mode—CRC4 Framing Structure

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0x66
0x8009	TPCR1	0x48
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x40
0x801D	E1RCR	0x20
0x801E	E1TCR	0x02
0x8001	IOCR1	0x80
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x00
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x00
0x8015	IMR1	0x00
0x8016	SR2	0x09
0x8017	IMR2	0x00
0x8018	SR3	0x44
0x8019	IMR3	0x00
0x801A	SR4	0x00

0x801B	IMR4	0x00
0x8021	SR5	0x00
0x8022	IMR5	0x00
0x8030	LIC1	0x01
0x8031	LIC2	0x18
0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0xFF
0x8057	RNAF	0xFF
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

Table 4. Register Settings for E1 Mode—FAS Framing Structure

Register Address	Register Name	Value
0x8010	IDR	0x22

0x8000	TSTRREG	0x00
0x8008	MCREG	0x44
0x8009	TPCR1	0x48
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x40
0x801D	E1RCR	0x20
0x801E	E1TCR	0x02
0x8001	IOCR1	0x80
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x00
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x00
0x8015	IMR1	0x00
0x8016	SR2	0x09
0x8017	IMR2	0x00
0x8018	SR3	0x44
0x8019	IMR3	0x00
0x801A	SR4	0x00
0x801B	IMR4	0x00
0x8021	SR5	0x00

0x8022	IMR5	0x00
0x8030	LIC1	0x01
0x8031	LIC2	0x18
0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0xFF
0x8057	RNAF	0xff
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

T1 Mode

The DS26504 supports unframed and framed T1 modes. This section provides detailed register settings for T1 unframed mode as well as those for the D4 and ESF framing structures.

Table 5. Register Settings for T1 Mode—Unframed

Register Address	Register Name	Value

0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0x11
0x8009	TPCR1	0x00
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x00
0x801D	E1RCR	0x00
0x801E	E1TCR	0x00
0x8001	IOCR1	0x00
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x0F
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x06
0x8015	IMR1	0x00
0x8016	SR2	0x03
0x8017	IMR2	0x00
0x8018	SR3	0x0C
0x8019	IMR3	0x00
0x801A	SR4	0x14
0x801B	IMR4	0x00

0x8021	SR5	0x00
0x8022	IMR5	0x00
0x8030	LIC1	0x03
0x8031	LIC2	0x00
0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0x00
0x8057	RNAF	0x00
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

Table 6. Register Settings for T1 Mode—Unframed

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00

0x8008	MCREG	0x00
0x8009	TPCR1	0x00
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x20
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0xC0
0x801D	E1RCR	0x00
0x801E	E1TCR	0x00
0x8001	IOCR1	0x00
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0xE3
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x00
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x00
0x8015	IMR1	0x00
0x8016	SR2	0x00
0x8017	IMR2	0x00
0x8018	SR3	0x0C
0x8019	IMR3	0x00
0x801A	SR4	0x14
0x801B	IMR4	0x00
0x8021	SR5	0x00
0x8022	IMR5	0x00

0x8030	LIC1	0x01
0x8031	LIC2	0x10
0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0x00
0x8057	RNAF	0x00
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

Table 7. Register Settings for T1 Mode—ESF Framing Structure

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0x11
0x8009	TPCR1	0x00

0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x00
0x801D	E1RCR	0x00
0x801E	E1TCR	0x00
0x8001	IOCR1	0x00
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x0F
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x06
0x8015	IMR1	0x00
0x8016	SR2	0x8B
0x8017	IMR2	0x00
0x8018	SR3	0x0E
0x8019	IMR3	0x00
0x801A	SR4	0x1D
0x801B	IMR4	0x00
0x8021	SR5	0x00
0x8022	IMR5	0x00
0x8030	LIC1	0x01
0x8031	LIC2	0x10

0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0x00
0x8057	RNAF	0x00
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

G.703 Synchronous Interface Mode

Table 8. Register Settings for G.703 2.048MHz Synchronization Interface Mode

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0x88
0x8009	TPCR1	0x48
0x800A	TPCR2	0x00

0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x40
0x801D	E1RCR	0x20
0x801E	E1TCR	0x02
0x8001	IOCR1	0x80
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0xFF
0x8051	TFDL	0x1c
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x02
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x02
0x8015	IMR1	0x00
0x8016	SR2	0x05
0x8017	IMR2	0x00
0x8018	SR3	0x1C
0x8019	IMR3	0x00
0x801A	SR4	0x1F
0x801B	IMR4	0x00
0x8021	SR5	0x00
0x8022	IMR5	0x00
0x8030	LIC1	0x01
0x8031	LIC2	0x18
0x8032	LIC3	0x00

0x8033	LIC4	0x00
0x8034	TLBC	0x00
0x8056	RAF	0xFF
0x8057	RNAF	0xFF
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0xFF
0x8059	RSiNAF	0xFF
0x805A	RRA	0xFF
0x805B	RSa4	0xFF
0x805C	RSa5	0xFF
0x805D	RSa6	0xFF
0x805E	RSa7	0xFF
0x805F	RSa8	0xFF
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

6312kHz Synchronization Interface Mode

Table 9. Register Settings for 6312kHz Synchronization Interface Mode

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0xBB
0x8009	TPCR1	0xF8
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00

0x8003	T1RCR1	0x00
0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x40
0x801D	E1RCR	0x00
0x801E	E1TCR	0x00
0x8001	IOCR1	0x00
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x0F
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x06
0x8015	IMR1	0x00
0x8016	SR2	0x0b
0x8017	IMR2	0x00
0x8018	SR3	0x0E
0x8019	IMR3	0x00
0x801A	SR4	0x1F
0x801B	IMR4	0x00
0x8021	SR5	0x00
0x8022	IMR5	0x00
0x8030	LIC1	0x03
0x8031	LIC2	0x10
0x8032	LIC3	0x00
0x8033	LIC4	0x00

0x8034	TLBC	0x00
0x8056	RAF	0x00
0x8057	RNAF	0x00
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

64kHz Composite Clock Mode

Table 10. Register Settings for 64kHz Composite Clock

Register Address	Register Name	Value
0x8010	IDR	0x22
0x8000	TSTRREG	0x00
0x8008	MCREG	0x99
0x8009	TPCR1	0x90
0x800A	TPCR2	0x00
0x8007	T1CCR	0x00
0x8003	T1RCR1	0x00

0x8004	T1RCR2	0x00
0x8005	T1TCR1	0x00
0x8006	T1TCR2	0x40
0x801D	E1RCR	0x20
0x801E	E1TCR	0x02
0x8001	IOCR1	0x80
0x8002	IOCR2	0x00
0x8020	LBCR	0x00
0x801F	BOCC	0x00
0x8050	RFDL	0x00
0x8051	TFDL	0x1C
0x8052	RFDLM1	0x00
0x8053	RFDLM2	0x00
0x8011	INFO1	0x0F
0x8012	INFO2	0x00
0x801C	INFO3	0x04
0x8013	IIR	0x00
0x8014	SR1	0x06
0x8015	IMR1	0x00
0x8016	SR2	0x08
0x8017	IMR2	0x00
0x8018	SR3	0x0C
0x8019	IMR3	0x00
0x801A	SR4	0x07
0x801B	IMR4	0x00
0x8021	SR5	0x00
0x8022	IMR5	0x00
0x8030	LIC1	0x01
0x8031	LIC2	0x18
0x8032	LIC3	0x00
0x8033	LIC4	0x00
0x8034	TLBC	0x00

0x8056	RAF	0x00
0x8057	RNAF	0x00
0x8040	TAF	0x1B
0x8041	TNAF	0x40
0x8058	RSiAF	0x00
0x8059	RSiNAF	0x00
0x805A	RRA	0x00
0x805B	RSa4	0x00
0x805C	RSa5	0x00
0x805D	RSa6	0x00
0x805E	RSa7	0x00
0x805F	RSa8	0x00
0x8042	TSiAF	0x00
0x8043	TSiNAF	0x00
0x8044	TRA	0x00
0x8045	TSa4	0x00
0x8046	TSa5	0x00
0x8047	TSa6	0x00
0x8048	TSa7	0x00
0x8049	TSa8	0x00
0x804A	TSACR	0x00

Related Parts	
DS26502	T1/E1/J1/64KCC BITS Element
DS26503	T1/E1/J1 BITS Element
DS26504	T1/E1/J1/64KCC BITS Element

More Information
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For Samples: https://www.maximintegrated.com/en/samples
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