

## SINGLE 3-INPUT POSITIVE OR-AND GATE

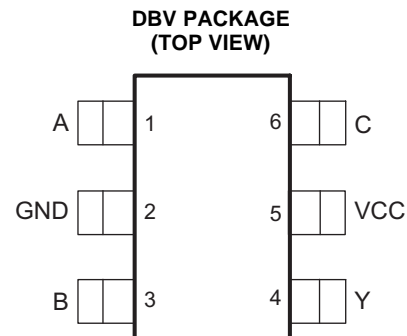
 Check for Samples: [SN74LVC1G3208-EP](#)

### FEATURES

- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5 ns at 3.3 V
- Low Power Consumption, 12.5- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input  
( $V_{hys} = 250$  mV Typ at 3.3 V)
- Can Be Used in Three Combinations:
  - OR-AND Gate
  - OR Gate
  - AND Gate
- $I_{off}$  Supports Partial-Power-Down Mode Operation

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Ranges <sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



(1) Custom temperature ranges available

### DESCRIPTION/ORDERING INFORMATION

This device is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G3208 is a single 3-input positive OR-AND gate. It performs the Boolean function  $Y = (A + B) \cdot C$  in positive logic.

By tying one input to GND or  $V_{CC}$ , the SN74LVC1G3208 offers two more functions. When C is tied to  $V_{CC}$ , this device performs as a 2-input OR gate ( $Y = A + B$ ). When A is tied to GND, the device works as a 2-input AND gate ( $Y = B \cdot C$ ). This device also works as a 2-input AND gate when B is tied to GND ( $Y = A \cdot C$ ).

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

$T_A$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOT (SOT-23) – DBV	Reel of 250	74LVC1G3208MDBVTEP	CDD5M	V62/13605-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



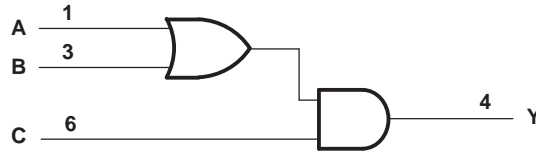
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE<sup>(1)</sup>**

INPUTS			OUTPUT Y
A	B	C	
H	X	H	H
X	H	H	H
X	X	L	L
L	L	H	L

(1) X = Valid H or L

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**FUNCTION SELECTION TABLE**

LOGIC FUNCTION	FIGURE
2-Input AND Gate	1
2-Input OR Gate	2
$Y = (A + B) \cdot C$	3

**LOGIC CONFIGURATIONS**

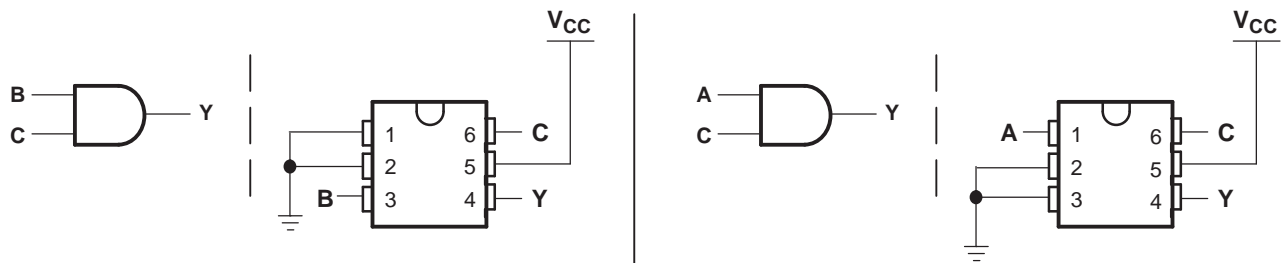


Figure 1. 2-Input AND Gate

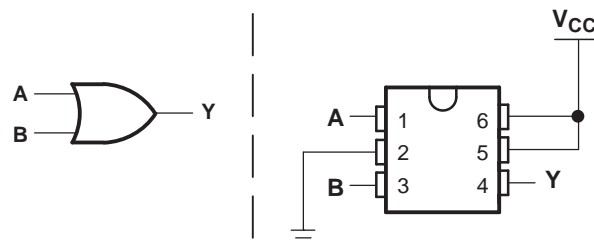


Figure 2. 2-Input OR Gate



Figure 3.  $Y = (A + B) \cdot C$

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage range	-0.5	6.5	V
$V_I$ Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$ Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$ Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$ Input clamp current		$V_I < 0$	-50 mA
$I_{OK}$ Output clamp current		$V_O < 0$	-50 mA
$I_O$ Continuous output current			±50 mA
Continuous current through $V_{CC}$ or GND			±100 mA
$T_{stg}$ Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	SN74LVC1G3208		UNITS
	DBV		
	6 PINS		
$\theta_{JA}$ Junction-to-ambient thermal resistance <sup>(2)</sup>	207		°C/W
$\theta_{JCTop}$ Junction-to-case (top) thermal resistance <sup>(3)</sup>	148.1		
$\theta_{JB}$ Junction-to-board thermal resistance <sup>(4)</sup>	50.6		
$\psi_{JT}$ Junction-to-top characterization parameter <sup>(5)</sup>	41.2		
$\psi_{JB}$ Junction-to-board characterization parameter <sup>(6)</sup>	50.1		
$\theta_{JCbott}$ Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

**Recommended Operating Conditions<sup>(1)</sup>**

			<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.4		
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	–4		mA
		V <sub>CC</sub> = 2.3 V	–8		
		V <sub>CC</sub> = 3 V	–16		
			–24		
		V <sub>CC</sub> = 4.5 V	–32		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		mA
		V <sub>CC</sub> = 2.3 V	8		
		V <sub>CC</sub> = 3 V	16		
			24		
		V <sub>CC</sub> = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V	10		
		V <sub>CC</sub> = 5 V ± 0.5 V	5		
T <sub>A</sub>	Operating free-air temperature		–55	125	°C

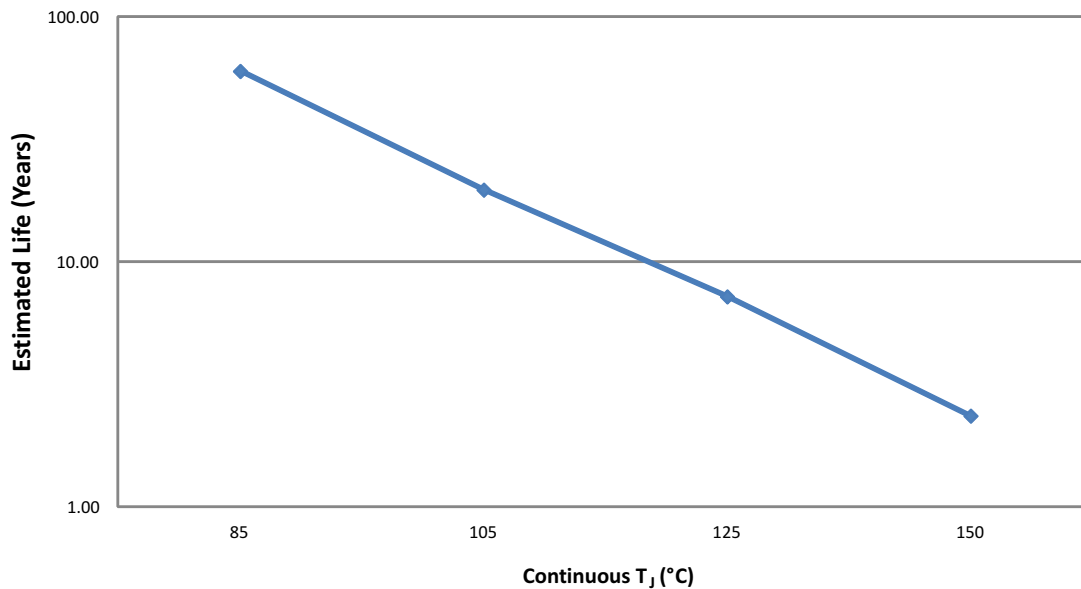
(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -8 mA	2.3 V	1.9			
	I <sub>OH</sub> = -16 mA	3 V	2.4			
	I <sub>OH</sub> = -24 mA		2.3			
	I <sub>OH</sub> = -32 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 5.5 V			0.11	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.52	
	I <sub>OL</sub> = 8 mA	2.3 V			0.45	
	I <sub>OL</sub> = 16 mA	3 V			0.68	
	I <sub>OL</sub> = 24 mA				1.1	
	I <sub>OL</sub> = 32 mA	4.5 V			1.1	
I <sub>I</sub>	A, B, or C inputs V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	-12.05		8.6	µA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	-22		41.5	µA
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND      I <sub>O</sub> = 0	1.65 V to 5.5 V			12.5	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V,    Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5		pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.



- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

**Figure 4. 74LVC1G3208-EP Operating Life Derating Chart**

### Switching Characteristics

only valid for -40°C to 85°C,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	3.7	14	2.5	7	1.7	5	1.3	3.4	ns

### Switching Characteristics

only valid for -40°C to 85°C,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	2.5	17.5	1.8	7.6	1.8	5.9	1.3	4.0	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 6](#))

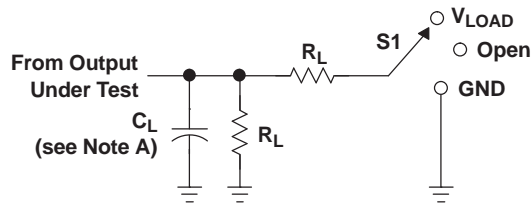
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y		17.5		7.6		5.9		4.5	ns

### Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	15	15	16	17	pF

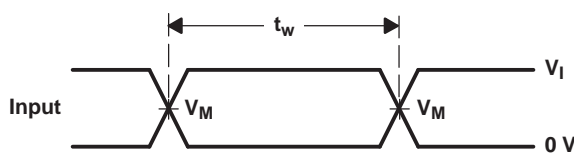
PARAMETER MEASUREMENT INFORMATION



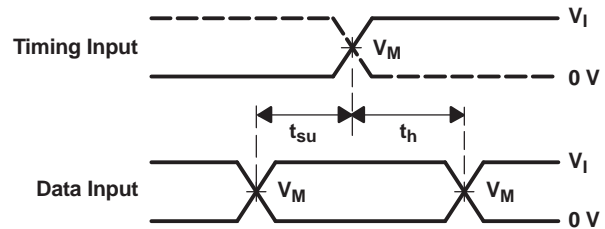
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

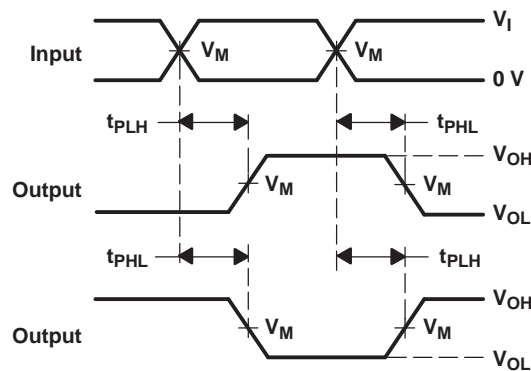
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V



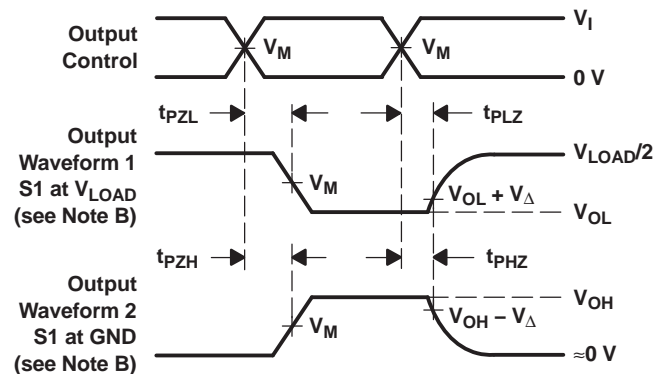
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

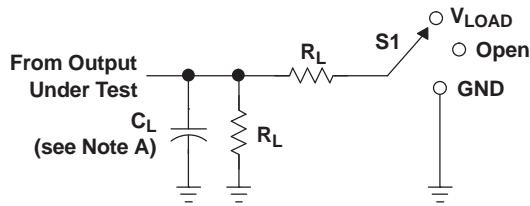


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

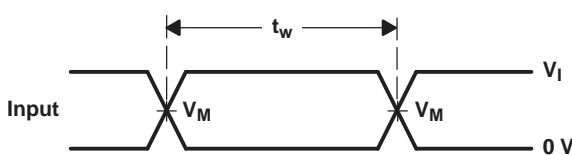
PARAMETER MEASUREMENT INFORMATION



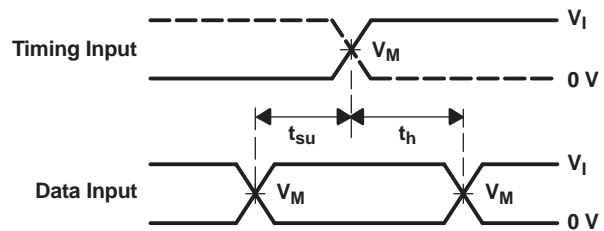
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

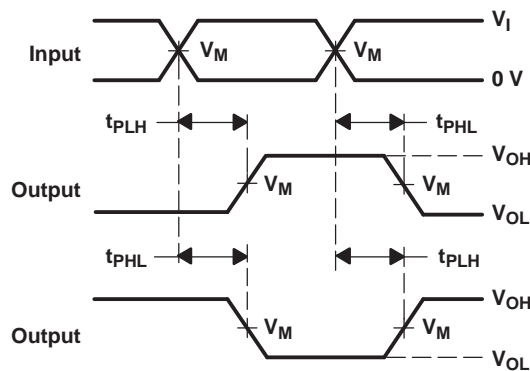
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



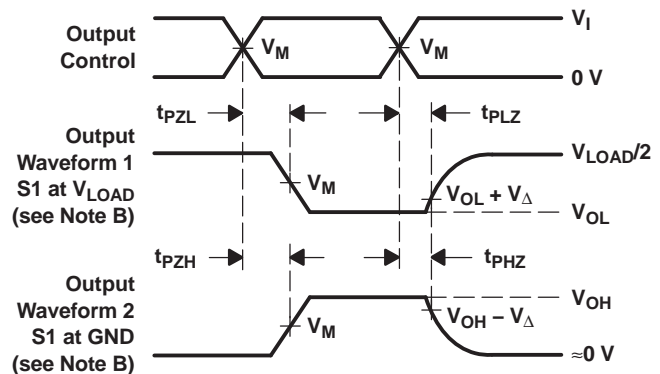
VOLTAGE WAVEFORMS PULSE DURATION



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  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 6. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G3208MDBVTEP	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CDD5M	<b>Samples</b>
V62/13605-01XE	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CDD5M	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G3208-EP :**

- Catalog: [SN74LVC1G3208](#)
- Automotive: [SN74LVC1G3208-Q1](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3208MDBVTEP	SOT-23	DBV	6	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3208MDBVTEP	SOT-23	DBV	6	250	180.0	180.0	18.0

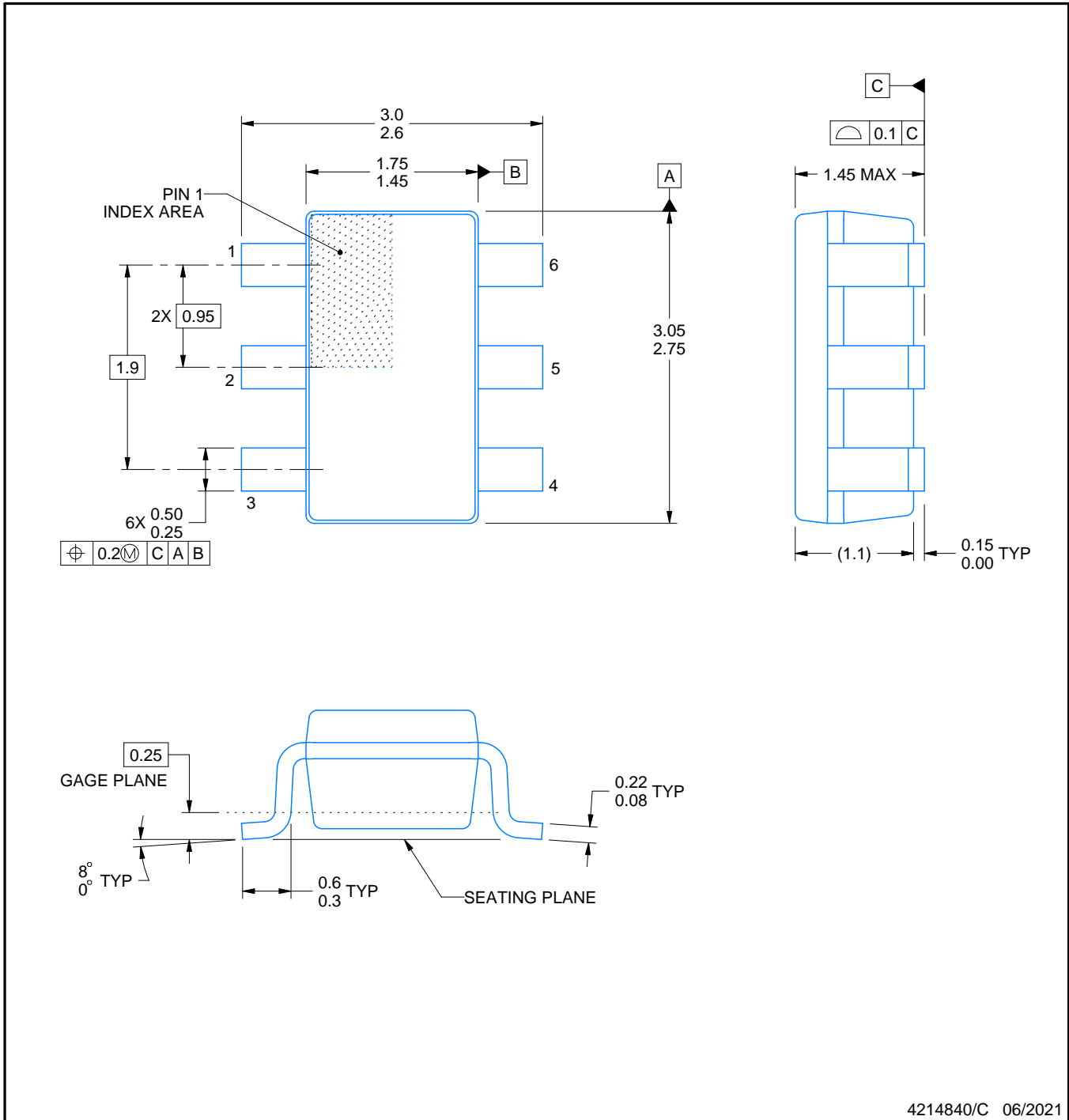
DBV0006A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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