

Notification Number:	20210914002	Notification Date:	September 29, 2021
Title:	Datasheet for MSP430FR247x		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



MSP430FR2476, MSP430FR2475

SLASE07C – MARCH 2019 – REVISED SEPTEMBER 2021

Changes from December 11, 2019 to September 14, 2021

Page

• Updated the numbering format for tables, figures, and cross references throughout the document.....	1
• Corrected the RAM size for the MSP430FR2475 throughout the document (changed from 4KB to 6KB).....	1
• Added links to online collateral in Section 3 Description	1
• Corrected the pin numbers for the Veref+ and Veref- signals in Table 7-2, Signal Descriptions	15
• Corrected the TAXRMP, USCIA0RMP, USCIB0RMP, and USCIB1RMP bit names in the notes for Table 7-2, Signal Descriptions	15
• Corrected the USCIA0RMP and USCIBxRMP bit names in Section 9.10.7, Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)	54
• Corrected the TAXRMP bit name in the notes for Table 9-16, TA2 and TA3 Pin Configurations of Remap Functionality	55
• Added an inverter to the Schmitt-trigger enable in Figure 9-4, Port Input/Output With Schmitt Trigger	64
• Corrected the value of the P5SEL.x column for P5.3 and P5.4 in Table 9-27, Port P5 (P5.0 to P5.7) Pin Functions	69
• Added the SYSCFG3 register to Table 9-35, SYS Registers (Base Address: 0140h)	74

The datasheet number will be changing.

Device Family	Change From:	Change To:
MSP430FR247x	SLASE07B	SLASE07C

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/MSP430FR2476>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None.

Product Affected:

MSP430FR2475TPT	MSP430FR2475TRHAT	MSP430FR2476TPT	MSP430FR2476TRHAT
MSP430FR2475TPTR	MSP430FR2475TRHBR	MSP430FR2476TPTR	MSP430FR2476TRHBR

MSP430FR2475TRHAR	MSP430FR2475TRHBT	MSP430FR2476TRHAR	MSP430FR2476TRHBT
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