SR70
RailClamp®
Low Capacitance TVS Diode Array

PROTECTION PRODUCTS - RailClamp®

Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR70 has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltages caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and **lightning**. The SR70 has been optimized for use on ADSL and other high-speed interfaces.

The unique design of the SR70 integrates four surge rated, low capacitance steering diodes in a low profile SOT-143 package. It has a typical capacitance of only 5pF and may be used to protect two high-speed lines without sacrificing signal integrity. The SR70 is designed to replace "standard" rectifiers that are not rated for the high energy surges that are normally expected in telecommunications applications.

During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The maximum clamping voltage seen by the protected circuit will be one diode drop (V_F) above the supply (reference) voltage. The SR70 may be used as a stand alone device or in conjunction with TVS diodes for enhanced protection.

Features

- Transient protection for high speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 1kV, 24A (8/20µs)
- Array of surge rated, low capacitance diodes
- Protects two I/O lines
- Low capacitance (5pF typical) for high-speed interfaces
- Low clamping voltage
- Solid-state silicon-avalanche technology

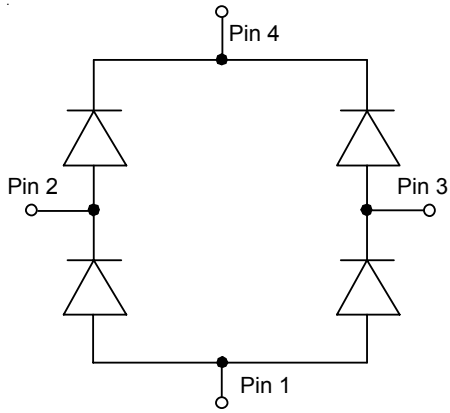
Mechanical Characteristics

- JEDEC SOT-143 package
- UL 497B listed
- Molding compound flammability rating: UL 94V-0
- Marking: R70
- Packaging: Tape and Reel per EIA 481

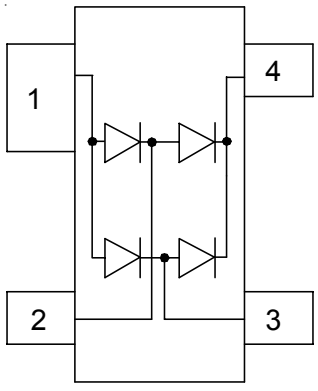
Applications

- ADSL Lines
- I^2C Bus Protection
- Video Line Protection
- T1/E1 secondary IC Side Protection
- Portable Electronics
- Microcontroller Input Protection
- WAN/LAN Equipment
- ISDN S/T Interface

Circuit Diagram



Schematic & PIN Configuration



SOT-143 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current (t_p = 8/20µs)	I_{PP}	24	A
Rectifier Repetitive Peak Reverse Voltage	V_{RRM}	70	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

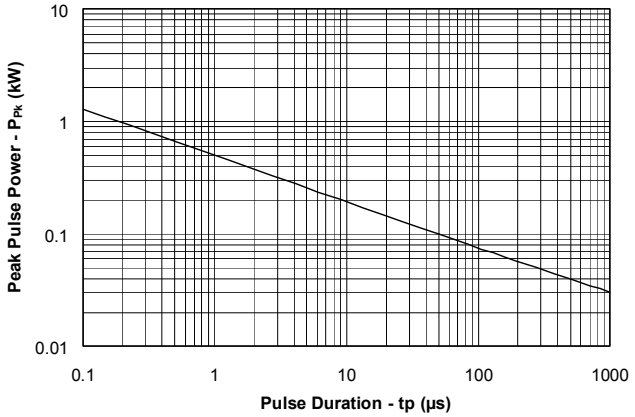
Electrical Characteristics (T=25°C)

SR70

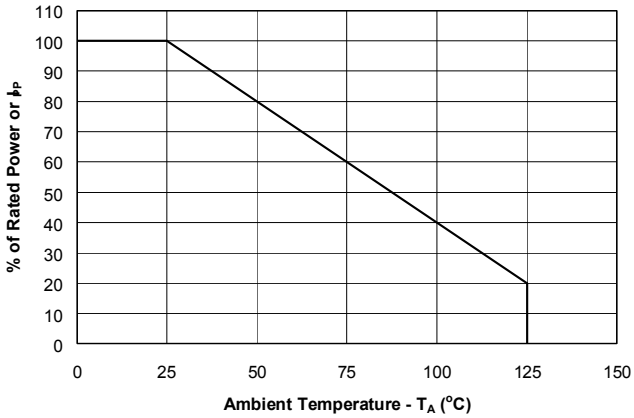
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Peak Reverse Stand-Off Voltage	V_{RRM}				70	V
Reverse Breakdown Voltage	V_{BR}	I_t = 50µA	85			V
Reverse Leakage Current	I_R	V_{RWM} = 70V, T=25°C			5	µA
Forward Clamping Voltage	V_{FC}	I_{PP} = 1A, t_p = 8/20µs			1.5	V
Forward Clamping Voltage	V_{FC}	I_{PP} = 10A, t_p = 8/20µs			3.3	V
Forward Clamping Voltage	V_{FC}	I_{PP} = 24A, t_p = 8/20µs			7	V
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		5	10	pF
		Between I/O pins V_R = 0V, f = 1MHz		3		pF

Typical Characteristics

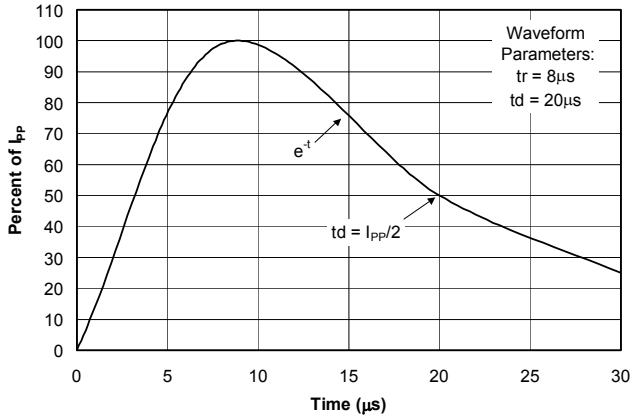
Non-Repetitive Peak Pulse Power vs. Pulse Time



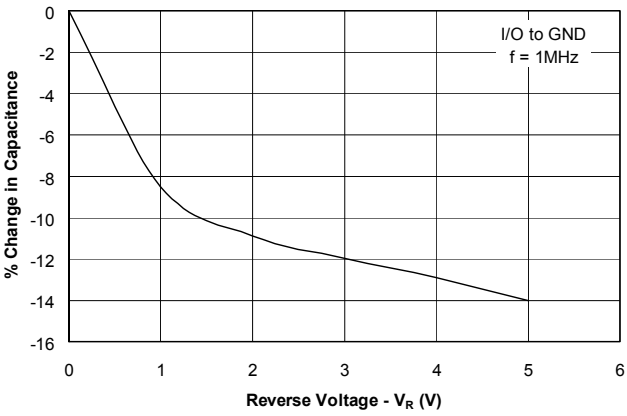
Power Derating Curve



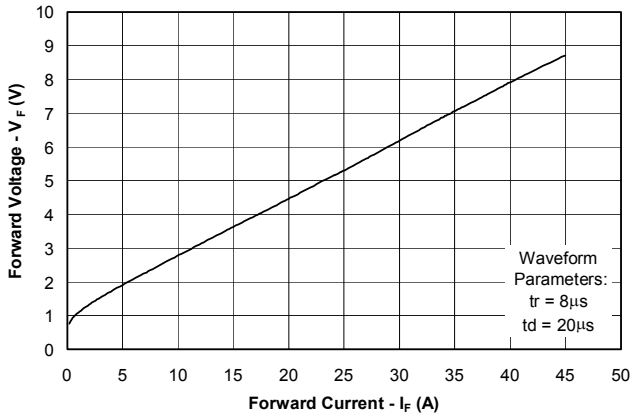
Pulse Waveform



Capacitance vs. Reverse Voltage



Forward Voltage vs. Forward Current



Applications Information

Device Connection Options for Protection of Two High-Speed Data Lines

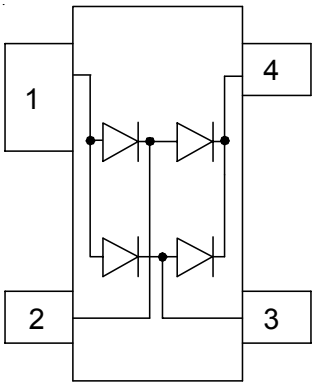
The SR70 is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2 and 3. The negative reference (REF1) is connected at pin 1. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.
The positive reference (REF2) is connected at pin 4. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pins 2 and 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. An external TVS diode may be added between the supply rail and ground in order to prevent over-voltage on the supply rail.
2. In applications where no positive supply reference is available, or complete supply isolation is desired, an external TVS diode may be used as the reference. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

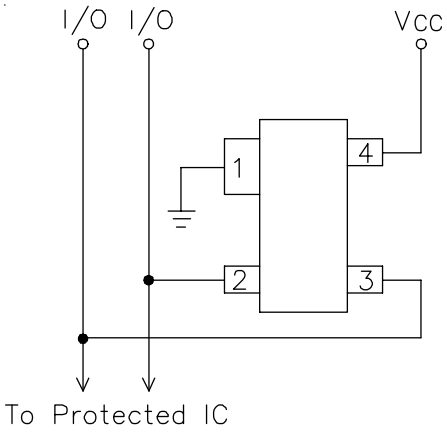
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

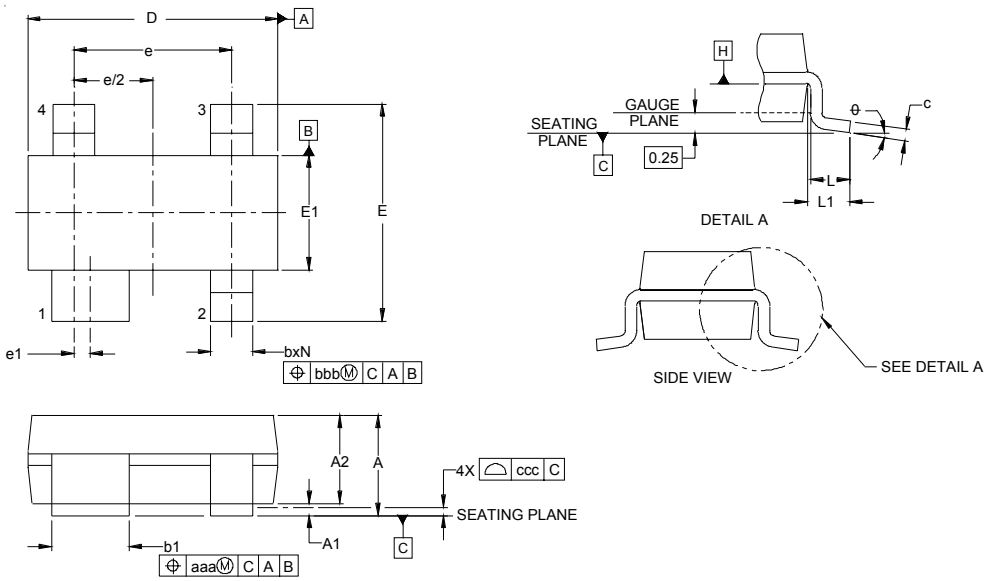
SR70 Pin Configuration



Data Line and Power Supply Protection Using Vcc as reference



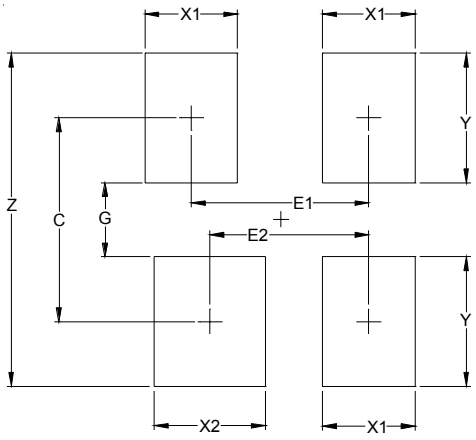
Outline Drawing - SOT-143



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.048	0.80	-	1.22
A1	.000	-	.006	0.013	-	0.15
A2	.029	.035	.042	0.75	0.90	1.07
b	.011	-	.020	0.30	-	0.51
b1	.029	-	.037	0.76	-	0.94
c	.003	-	.008	0.08	-	0.20
D	.110	.114	.120	2.80	2.90	3.04
E	.082	.093	.104	2.10	2.37	2.64
E1	.047	.051	.055	1.20	1.30	1.40
e	.075			1.92 BSC		
e1	.008			0.20 BSC		
L	.015	.020	.024	0.40	0.50	0.60
L1	(.021)			(0.54)		
N	4			4		
θ	0°	-	8°	0°	-	8°
aaa	.006			0.15		
bbb	.008			0.20		
ccc	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD TO-253, VARIATION D.

Land Pattern - SOT-143

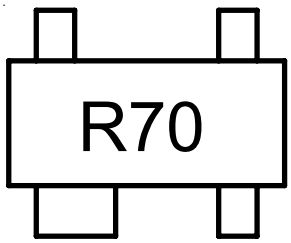


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.087)	(2.20)
E1	.076	1.92
E2	.068	1.72
G	.031	0.80
X1	.039	1.00
X2	.047	1.20
Y	.055	1.40
Z	.141	3.60

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A.

Marking Codes

Part Number	Marking Code
SR70	R70



SR70 Marking (Top View)

Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SR70.TC	SnPb	3,000	7 Inch
SR70.TCT	Pb Free	3,000	7 Inch

Lead-free version is RoHS/WEEE Compliant

Contact Information

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