EN6382QI 8A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN6382QI is an Intel® Enpirion® Power System on a Chip (PowerSoC) DC-DC converter with an integrated inductor, PWM controller, MOSFETsF and compensation to provide the smallest solution size in an 8x8x3mm 56 pin QFN module. It offers very high efficiency and is able to provide 8A continuous output current with no de-rating. The EN6382QI also provides excellent line and load regulation over temperature. The EN6382QI is specifically designed to meet the precise voltage and fast transient requirements of high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architecture.

Other features include precision enable threshold, pre-bias monotonic start-up, and programmable soft-start. The device's advanced circuit techniques, ultra-high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra-compact DC-DC conversion.

Intel Enpirion integrated inductor solution significantly helps to reduce noise. The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements. All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- High Efficiency (Up to 96%)
- Excellent Ripple and EMI Performance
- Up to 8A Continuous Operating Current
- Input Voltage Range (3.0V to 6.5V)
- 1.5% V_{FB} Accuracy
- Optimized Total Solution Size (160 mm^2)
- Precision Enable Threshold for Sequencing
- Programmable Soft-Start
- Pin compatible with the EN6362QI (6A)
- Thermal, Over-Current, Short Circuit, Reverse Current Limit and Under-Voltage Protections
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- Point of Load Regulation for FPGAs, ASICs Processors, DSPs, and Distributed Power Architectures
- Industrial automation, servers, storage, adapter cards, wireless base stations, test and measurement, and embedded computing.
- Space constrained applications that require the highest power density.
- Noise sensitive applications.

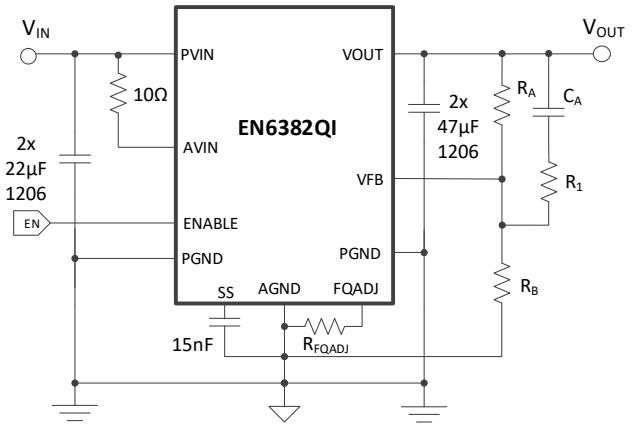


Figure 1: Simplified Applications Circuit

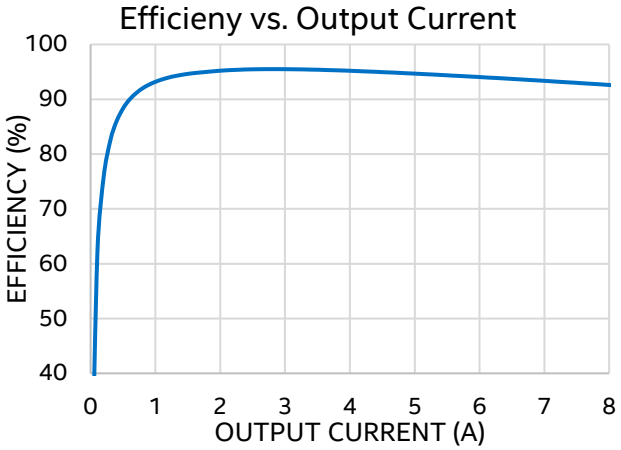


Figure 2: Efficiency at VIN = 5V, VOUT = 3.3V

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN6382QI	EN6382QI	-40°C to +125°C	56-pin (8mm x 8mm x 3mm) QFN
EVB-EN6382QI	EN6382QI	QFN Evaluation Board	

Packing and Marking Information:
https://www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

PIN FUNCTIONS

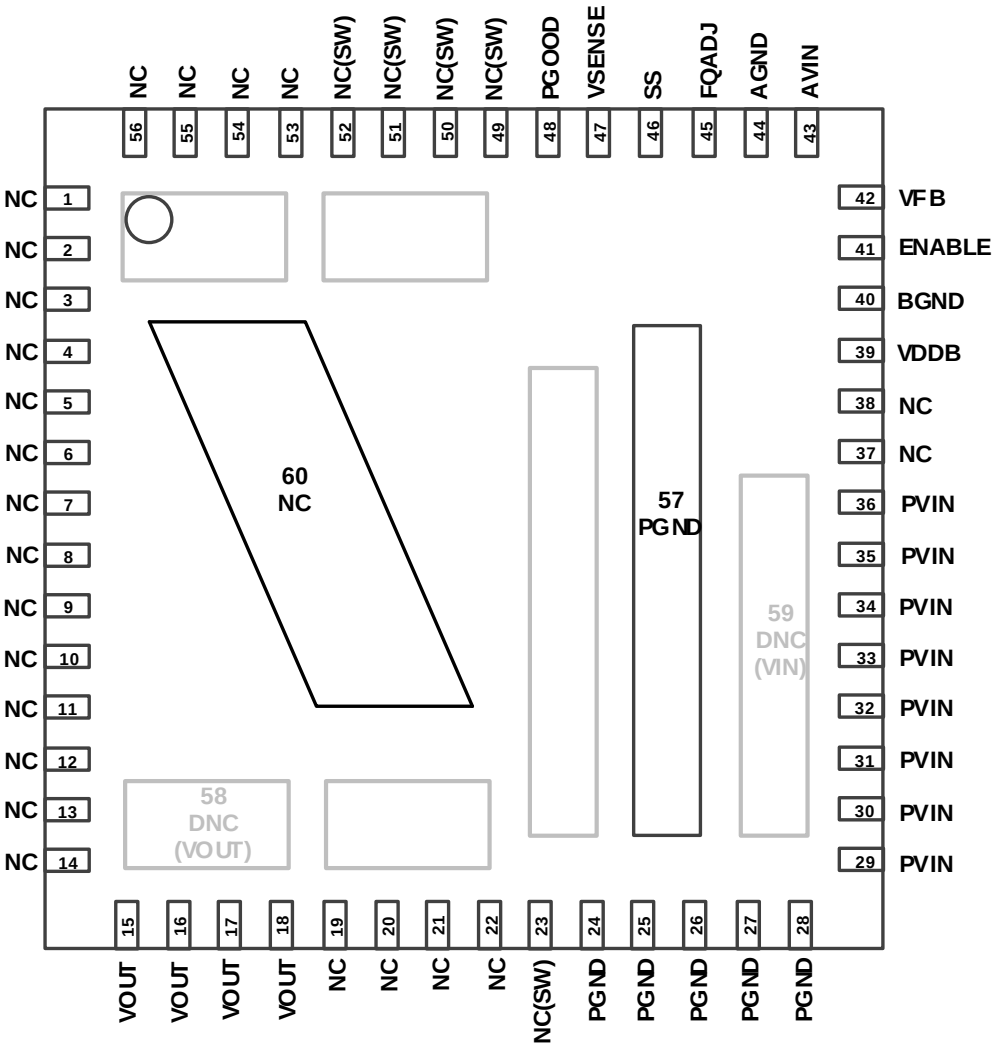


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

NOTE C: Grayed-out pins are not to be soldered to the PCB. Refer to Figure for the keepout diagram.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1-14, 19-22, 37-38, 53-56	NC	-	NO CONNECT: They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage. (1)
15-18	VOUT	Power	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins.
23	NC(SW)	-	NO CONNECT (1)
24-28	PGND	Power	Input and output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. Refer to VOUT, PVIN descriptions and Layout Recommendation for more details.
29-36	PVIN	Power	Input power supply. Connect to input power supply and place input filter capacitor(s) between these pins and PGND pins.
39	VDDB	Power	Internal regulated voltage used for the internal control circuitry. No external connection needed.
40	BGND	Power	Ground for VDDB. Refer to the pin 39 description.
41	ENABLE	Analog	Device enable pin. A high level or floating this pin enables the device while a low level disables the device. A voltage ramp from another power converter may be applied for precision enable. Refer to Power Up Sequencing.
42	VFB	Analog	This is the external feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) and resistor (R_C) are required parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage equal to 0.600V.
43	AVIN	Power	Analog input voltage for the control circuits. Connect this pin to the input power supply (PVIN) at a quiet point, through a 10Ω resistor.
44	AGND	Power	The quiet ground for the control circuits. Connect to the ground plane with a via right next to the pin.
45	FQADJ	Analog	Frequency adjust pin. This pin must have a resistor to AGND, which sets the free running frequency of the internal oscillator.
46	SS	Analog	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval. Refer to Soft-Start in the Functional Description for more details.
47	VSENSE	Analog	This pin senses output voltage. Connect VSENSE to VOUT.
48	PGOOD	Digital	PGOOD is a logic level high when VOUT is within -10% to +10% of the programmed output voltage ($0.9V_{OUT\_NOM} \le V_{OUT} \le 1.1V_{OUT\_NOM}$). This pin has an internal pull-up resistor to AVIN with a nominal value of 100kΩ.

PIN	NAME	TYPE	FUNCTION
49-52	NC (SW)	-	NO CONNECT: These pins must be soldered to PCB and can be electrically connected to each other but not to any external signal, voltage or ground. Failure to follow this guideline may result in device damage.
57	PGND	Power	Not a perimeter pin. Device thermal pad must be connected to the system GND plane for heat-sinking purposes. Refer to Layout Recommendation section.
58	DNC (VOUT)	Power	DO NOT CONNECT: Not a perimeter pin. This pin may be internally connected and must not be soldered to the PCB or connected to any external signal, voltage or ground.
59	DNC (VIN)	Power	DO NOT CONNECT: Not a perimeter pin. This pin may be internally connected and must not be soldered to the PCB or connected to any external signal, voltage or ground.
60	NC	-	Not a perimeter pin. Device mechanical pad must be soldered to the PCB to improve Board Level Reliability. This pin may be internally connected and must not be connected to any external signal, voltage or ground. (1)

(1) The NC pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	7.0	V
ENABLE, PGOOD		-0.3	V_{IN}+0.3	V
VFB, SS, FQADJ		-0.3	2.5	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.5	6.5	V
Output Voltage Range	V_{OUT}	0.6	$V_{IN} - V_{DO}$ (2)	V
Output Current Range	I_{OUT}		8	A
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	25	°C
Thermal Resistance: Junction to Ambient (0 LFM) (3)	θ_{JA}	16	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

(2) V_{DO} (dropout voltage) is defined as (I_{LOAD} x Droput Resistance). Please refer to Electrical Characteristics Table.

(3) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = 6.5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

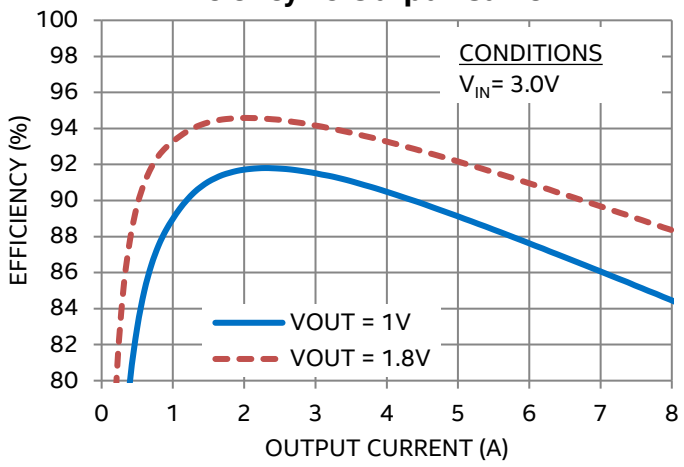
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VFB Pin Voltage	V_{FB}	T_A =-40°C to 85°C, 3V ≤ V_{IN} ≤ 6.5V, I_{LOAD} = 0A to 8A	0.591	0.600	0.609	V
	V_{UVLOR}	T_A =-40°C to 105°C, 3V ≤ V_{IN} ≤ 6.5V, I_{LOAD} = 0A to 8A	0.588	0.600	0.612	V
VFB Pin Input Leakage Current	I_{VFB}	VFB Pin Input Leakage Current	-10		+10	nA
Shut-Down Supply Current	I_{SD}	Power Supply Current with ENABLE=0		0.6		mA
Under Voltage Lock-out (V_{IN} Rising)	V_{UVLOR}	Voltage Above Which UVLO is Not Asserted		2.3		V
Under Voltage Lock-out (V_{IN} Falling)	V_{UVLOF}	Voltage Below Which UVLO is Asserted		2.0		V
Drop Out Voltage	V_{DO}	V_{IN} = 3V, V_{OUT} set 3.3V, I_{LOAD} = 8A, 100% duty cycle		280	600	mV
Drop Out Resistance	R_{DO}	Input to Output Resistance		35	75	mΩ
Over Current Trip Level	I_{OCP}	Sourcing Current	11	16	20	A
Switching Frequency	F_{SW}	R_{FQADJ} = 15kΩ, V_{IN} = 5V	1.15	1.5	1.7	MHz
Power Good Low		Range of Output Voltage as a Fraction of Programmed Value. PGOOD is Asserted. (4)	86	90	93.5	%
Power Good High		Range of Output Voltage as a Fraction of Programmed Value. PGOOD is Asserted. (4)	105	112	114.5	%
V_{PGOOD} Logic Level Low		With 4mA Current Sink into PGOOD Pin			0.2	V
V_{PGOOD} Logic Level High				V_{IN}		V
PGOOD Internal pull-up resistor				100		kΩ

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start Current	I_{SS}	Soft start current generator towards GND	6.5	9	11.5	µA
ENABLE Logic Level	V_{ENABLE}	3.0V ≤ V_{IN} ≤ 6.5V;	1.08	1.12	1.16	V
DISABLE Logic Level	$V_{DISABLE}$		0.95	1.01	1.07	V
ENABLE hysteresis	V_{EN_Hyst}			110		mV
Pull-up EN resistor	R_{EN_UP}			190		kΩ
Pull-down EN resistor	R_{EN_DWN}			110		kΩ
OTP level	T_{OTP}			150		°C
OTP hysteresis	OTP_{HYST}			25		°C

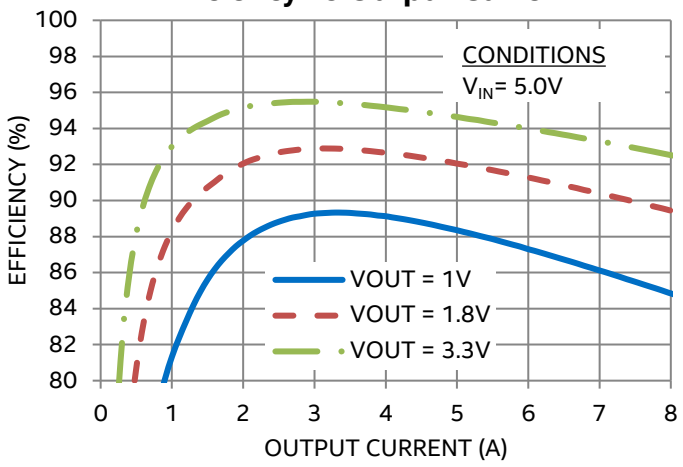
(4) After crossing the PGOOD threshold level, there is a 63 µs (at 1.5 MHz) delay before PGOOD is de-asserted.

TYPICAL PERFORMANCE CURVES

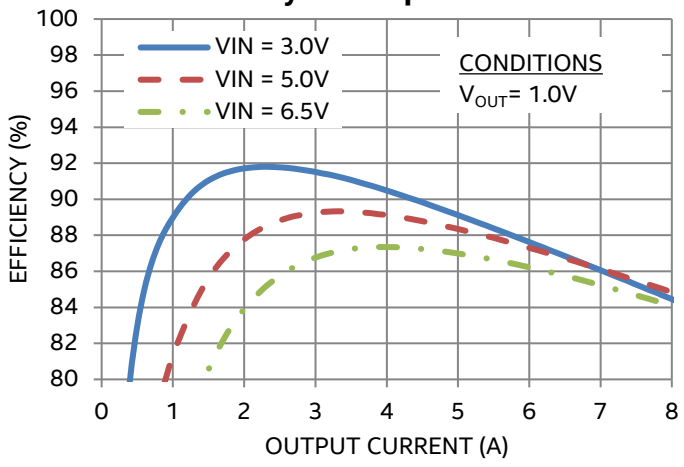
Efficiency vs Output Current



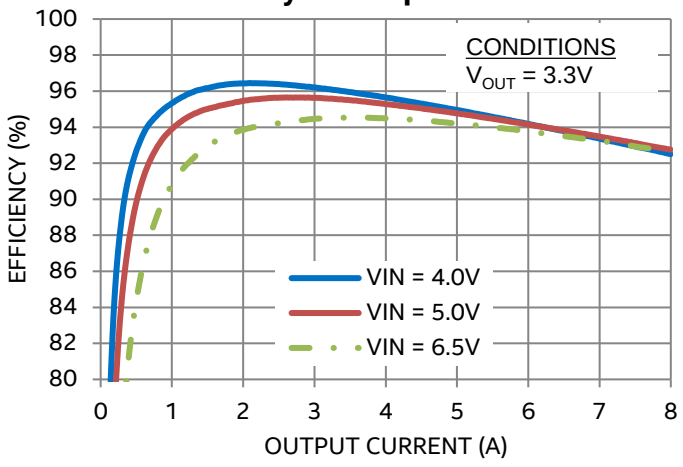
Efficiency vs Output Current



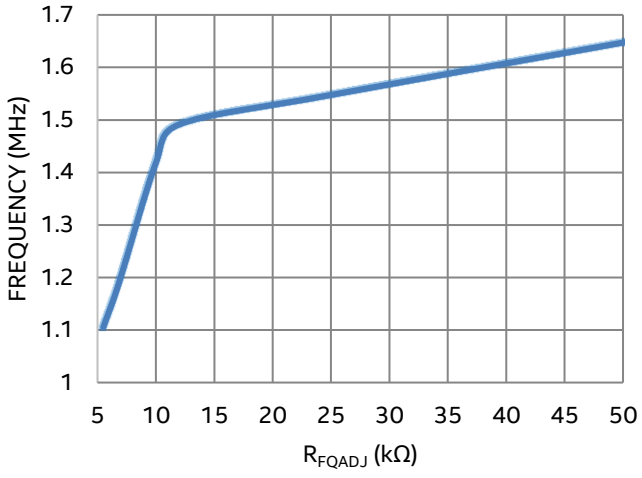
Efficiency vs Output Current



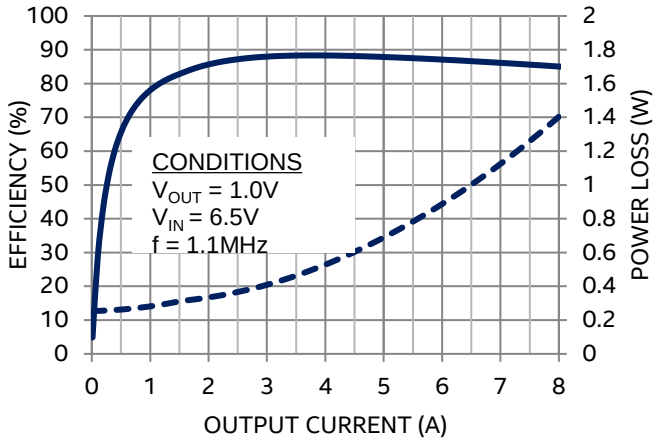
Efficiency vs Output Current



Frequency vs R_{FQADJ}

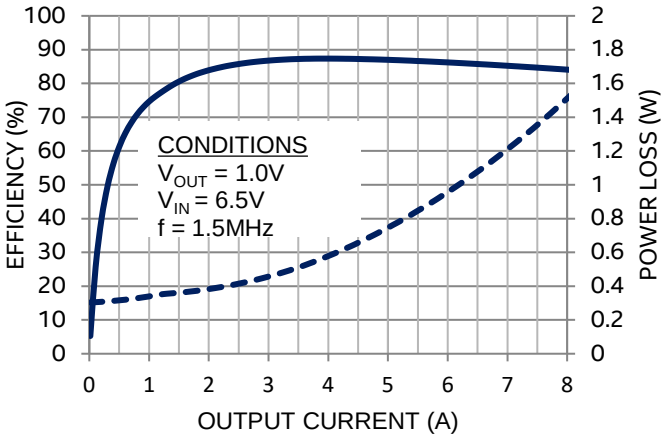


Efficiency, Power Loss vs Output Current

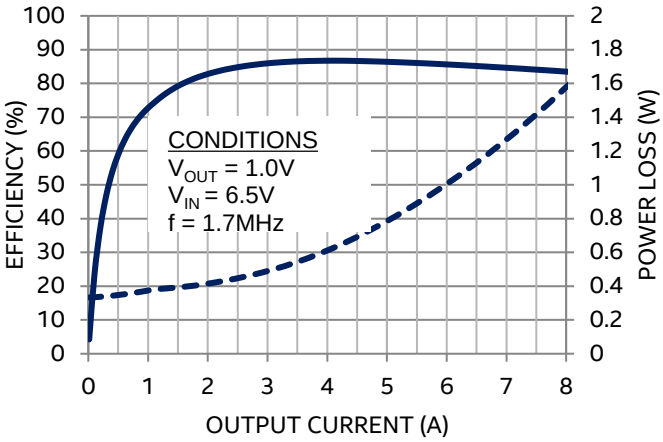


TYPICAL PERFORMANCE CURVES (CONTINUED)

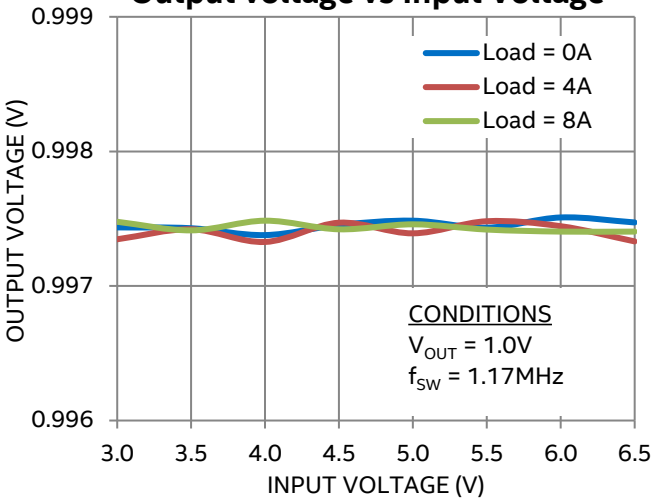
Efficiency, Power Loss vs Output Current



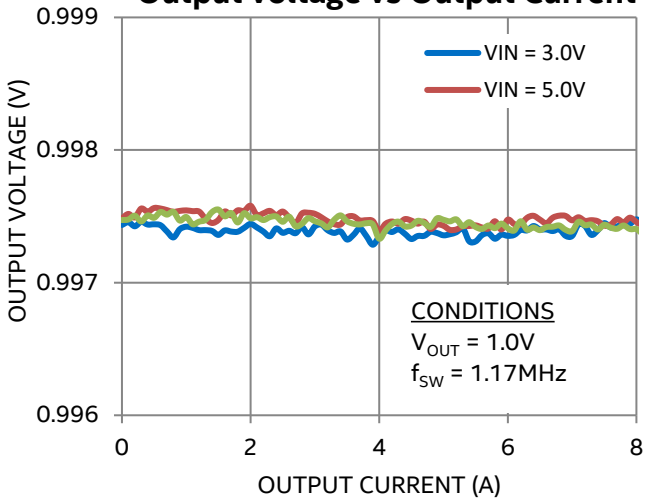
Efficiency, Power Loss vs Output Current



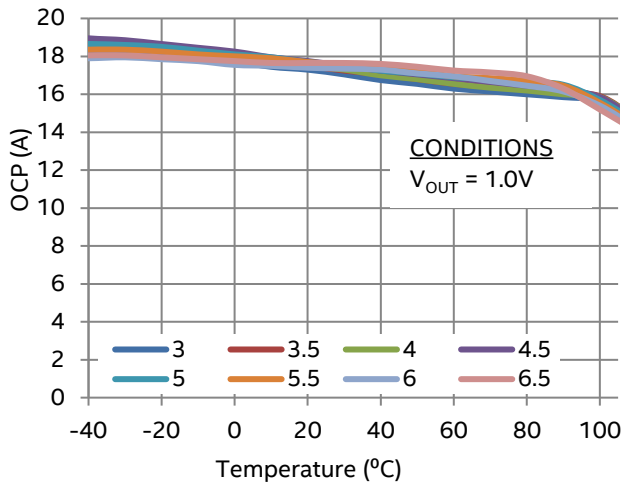
Output voltage vs Input Voltage



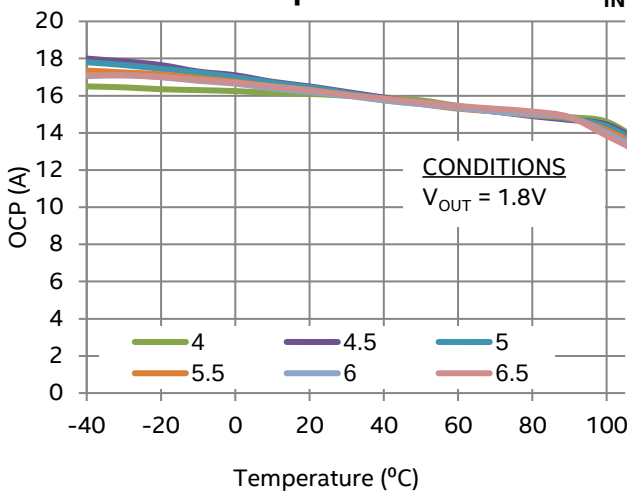
Output voltage vs Output Current



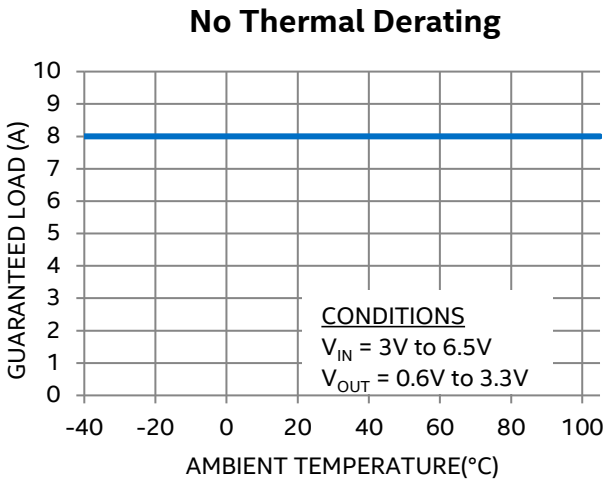
OCP vs Temperature at various V_{IN}



OCP vs Temperature at various V_{IN}

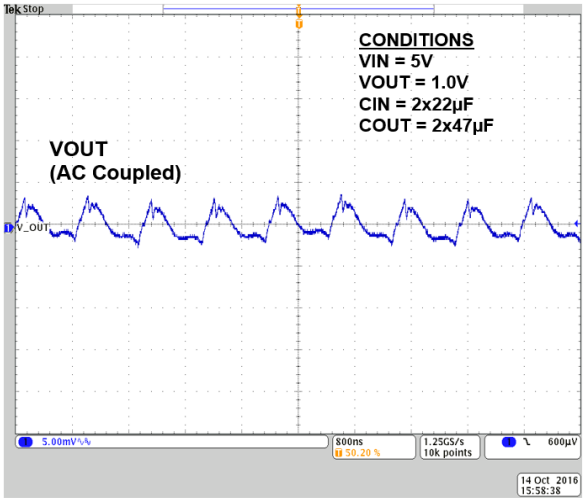


TYPICAL PERFORMANCE CURVES (CONTINUED)

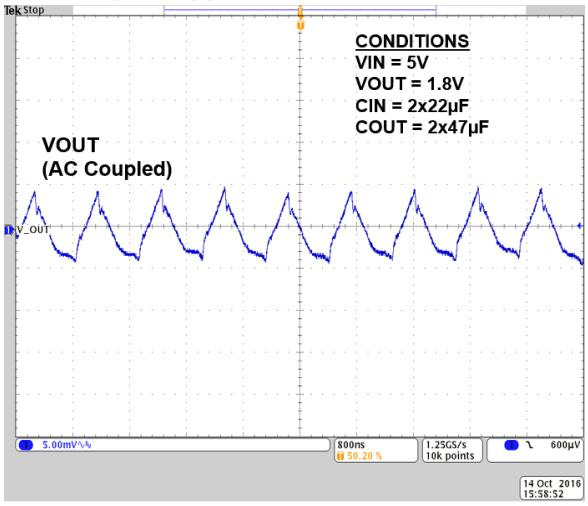


TYPICAL PERFORMANCE CHARACTERISTICS

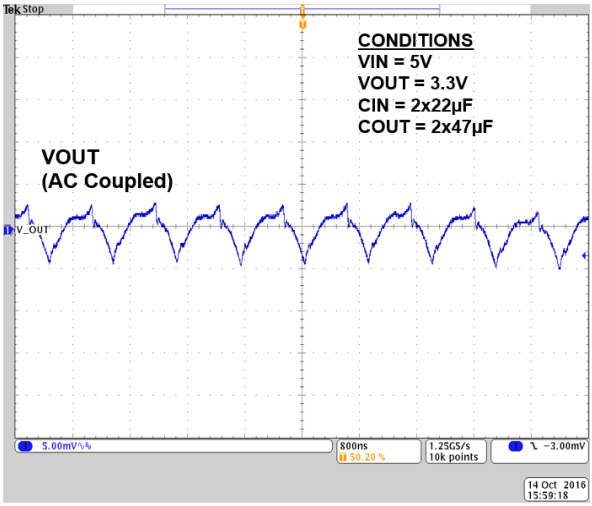
Output Ripple at 20MHz Bandwidth



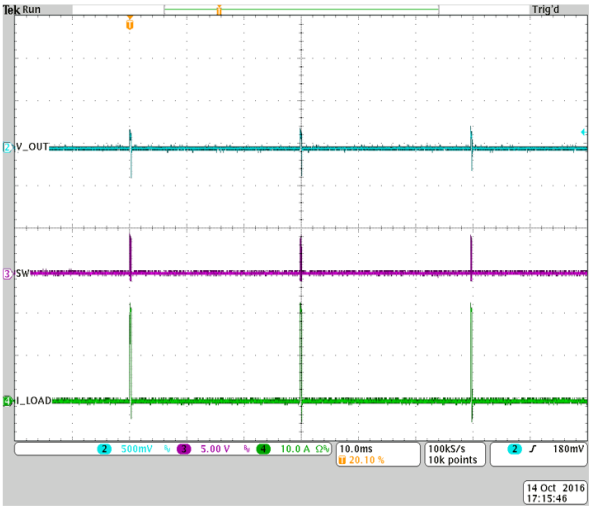
Output Ripple at 20MHz Bandwidth



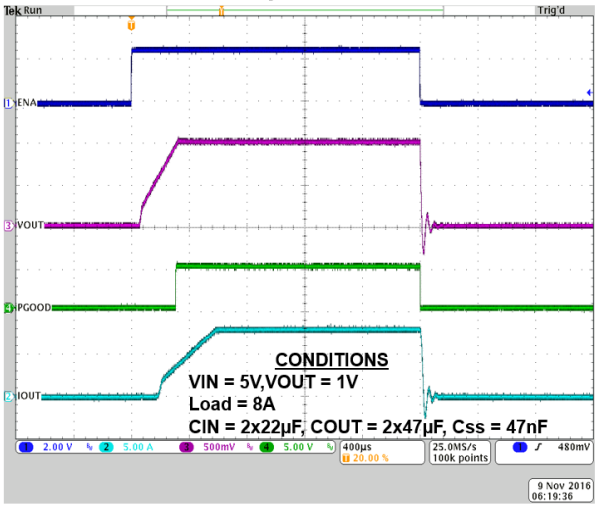
Output Ripple at 20MHz Bandwidth



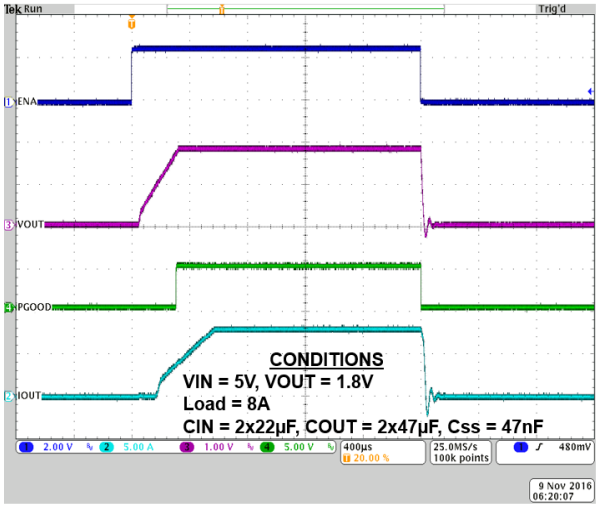
Hiccup mode during short-circuit protection



Startup Waveform

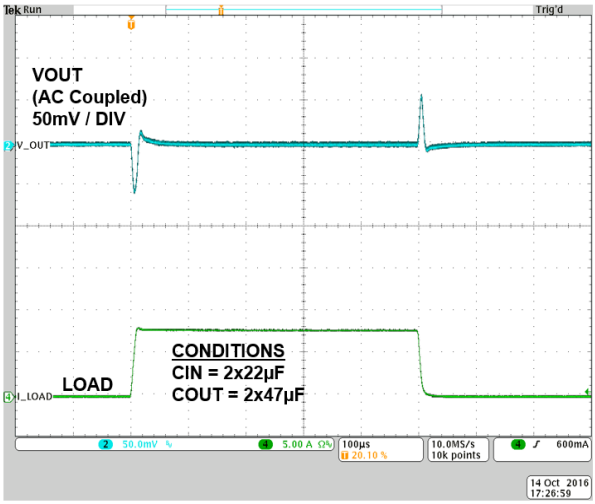


Startup Waveform

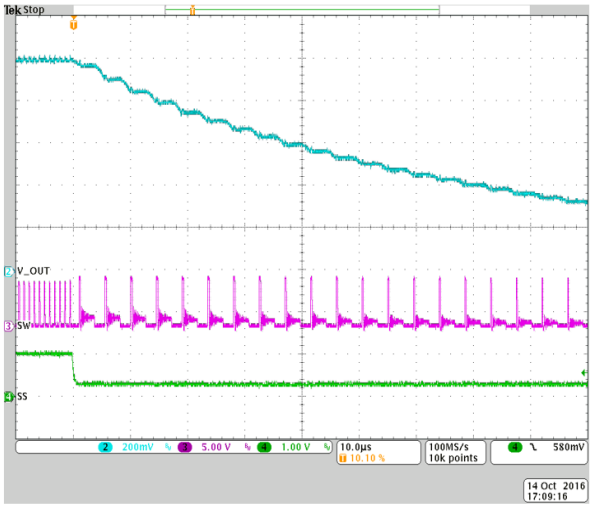


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Load Transient from 0A to 8A



Reverse current protection activated by forcing SS pin



FUNCTIONAL BLOCK DIAGRAM

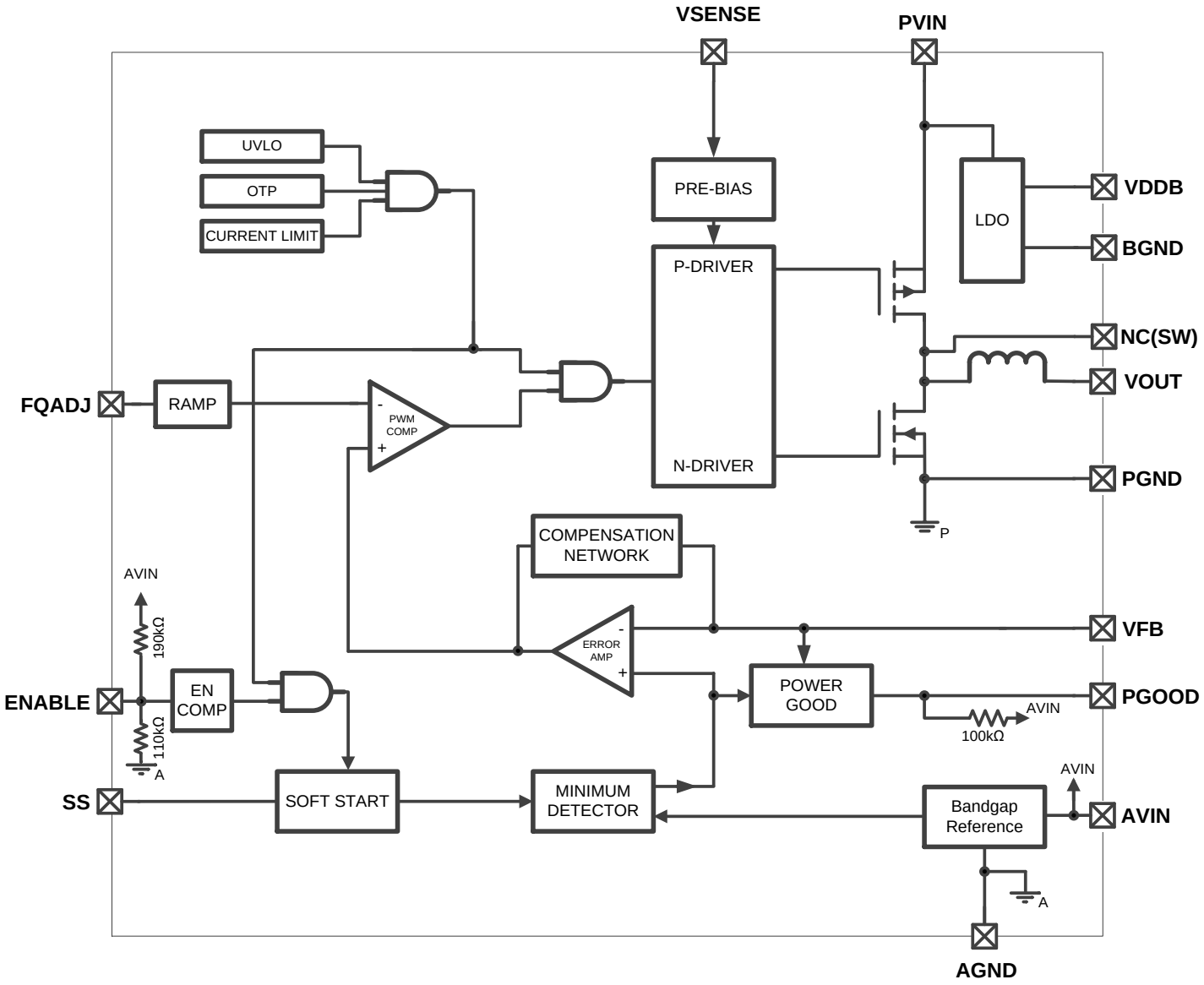


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN6382QI is a synchronous buck power supply with integrated power MOSFET switches and integrated inductor. The switching supply uses voltage mode control and a low noise PWM topology. The nominal input voltage range is 3.0 - 6.5 volts. The output voltage is programmed using an external resistor divider network. The feedback control loop incorporates a type IV voltage mode control design. Type IV voltage mode control maximizes control loop bandwidth and maintains excellent phase margin to improve transient performance. Although the EN6382QI is guaranteed to support up to 8A continuous output current operation over the full ambient temperature range (thermal design), the peak current supported before reaching OCP is substantially higher, exceeding 11A. The operating switching frequency can be adjusted by an external resistor between 1.1MHz and 1.7MHz. The high switching frequency enables the use of small-size input and output capacitors.

EN6382QI electrical features at a glance:

- Precision Enable Threshold
- Soft-Start
- Pre-bias Start-Up
- Resistor Programmable Switching Frequency
- Power Good
- Over-Current/Short Circuit Protection
- Reverse Current Limit (RCL)
- Thermal Shutdown (OTP) with Hysteresis
- Under-Voltage Lockout

Precision Enable

The ENABLE threshold is a precision analog voltage rather than a digital logic threshold. A precision voltage reference and a comparator circuit are kept powered up even when ENABLE is de-asserted. The narrow voltage gap between ENABLE Logic Low and ENABLE Logic High (about 100mV hysteresis) allows the device to turn on at a precise enable voltage level. The precise enable threshold, in conjunction with the proper choice of soft-start capacitors allows accurate sequencing for multiple power supplies. ENABLE has a 2ms lockout time that prevents the device from re-enabling immediately after it has been disabled.

Soft-Start

The SS pin, in conjunction with a small external capacitor between this pin and AGND provides the soft-start function, designed to limit in-rush current during start-up. When the part is enabled, soft-start (SS) current generator charges the SS capacitor in a linear manner. As long as the SS voltage level is smaller than the feedback reference (about 0.6V) the SS voltage is used as feedback reference, ensuring a linear increase of the output voltage. Once the voltage on the SS capacitor reaches 0.6V, the minimum detector Figure 4 will select the bandgap reference as target, while the voltage across the SS capacitor will continue ramping up until it reaches about 1.5V. As the SS voltage slew rate depends on the SS capacitor, so does the output voltage.

The rise time is defined as the time needed by the output voltage to go from zero to 95% of the programmed value. The rise time (t_{RISE}) is given by the following equation:

t_{RISE} [ms] = C_{ss} [nF] x 0.065

The recommended range for the value of the SS capacitor is between 4.7nF and 100nF.

Pre-Bias Start-up

The EN6382QI supports startup into a pre-biased load. A proprietary circuit ensures the output voltage rises up from the pre-bias value to the programmed output voltage. Start-up is guaranteed to be monotonic for pre-bias voltages in the range of 20% to 75% of the programmed output voltage with a minimum pre-bias voltage of 300mV. Outside of the 20% to 75% range, the output voltage rise will not be monotonic. For this feature to work properly, the EN6382QI must be enabled after V_{IN} ramped up.

Resistor Programmable Frequency

The operation of the EN6382QI can be optimized by a proper choice of the R_{FQADJ} resistor.

If high efficiency is the most important factor, then a lower switching frequency should be selected. If a better transient response is the most important factor, a higher switching frequency should be selected.

The typical Frequency vs R_{FQADJ} relationship over the suggested range of R_{FQADJ} is shown in the typical performance curves.

PGOOD Operation

The PGOOD pin is used only to signal whether the output voltage is within the specified range. The PGOOD signal is asserted high when the rising output voltage exceeds 92% of the programmed output voltage.

If the output voltage falls outside the range (roughly 90% to 110%), PGOOD remains asserted for the de-glitch time (about 63µs at 1.5MHz switching frequency). After the de-glitch time, PGOOD is de-asserted. PGOOD is also de-asserted if the output voltage exceeds 110% of the programmed output voltage.

Over Current Protection

The current level is sensed through the High Side Switch. The OCP trip point is nominally set around 16A average current. When the sensed current exceeds the current limit level, both power FETs are turned off for the rest of the switching cycle. If for the next cycle the over-current condition is removed, the PWM operation will resume. In the event the OCP circuit trips at least 8 consecutive PWM cycles, the device enters a hiccup mode; the device is disabled for about 23ms and restarted with a normal soft-start. This cycle can continue indefinitely as long as the over current condition persists.

Over Temperature Protection

Temperature sensing circuits in the controller will disable operation when the junction temperature exceeds approximately 150°C. Once the junction temperature drops by approximatively 25°C, the converter will resume operation with a normal soft-start.

Input Under-Voltage Lock-Out

When the rising input voltage is below the required voltage level (V_{UVLOR}), switching is inhibited; the lock-out threshold has hysteresis to prevent chatter, thus when the device is operating around the UVLO limit, the input voltage has to fall below the lower threshold (V_{UVLOF}) for the device to stop switching.

Reverse Current Limit protection

In order to prevent excessive current buildup in the low side MOSFET, a Reverse Current Limit protection is used; if the Low side MOSFET is kept on during two full PWM cycles, the output will be left floating for the next three cycles. This is an effective method of protecting the low side MOSFET against Over-Current during boost-back.

APPLICATION INFORMATION

Output Voltage Programming and loop Compensation

The EN6382QI output voltage is programmed using a simple resistor divider network. A phase lead capacitor plus a resistor are required for stabilizing the loop. Figure 5 shows the required components and the equations to calculate their values.

The EN6382QI output voltage is determined by resistor divider between VOUT and AGND with the midpoint going to VFB. During steady state operation, the voltage presented at the VFB pin is equal to the internal voltage reference.

Most of EN6382QI compensation network is integrated; however, a phase lead capacitor and a resistor are required in parallel with the upper resistor of the external feedback network.

Total compensation is optimized for use with two 47µF output capacitors and will result in a wide loop bandwidth and excellent load transient performance for most applications. Additional capacitance may be placed beyond the voltage sensing point outside the control loop. Voltage mode operation provides high noise immunity at light load.

In some cases, modifications to the compensation or output capacitance may be required to optimize device performance such as transient response, ripple, or hold-up time. The EN6382QI provides the capability to modify the control loop response to allow for customization for such applications. A simulation model is available upon request.

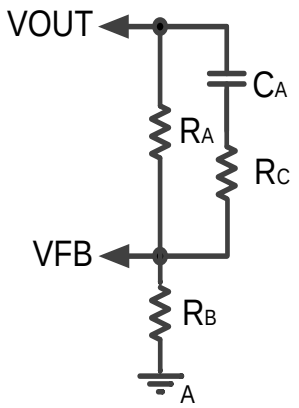


Figure 5: External Feedback/Compensation Network

The feedback and compensation network values depend on the input voltage and output voltage. The external feedback and compensation network values can be calculated using the equations below.

$$R_A = 294k\Omega$$

$$R_B = \frac{V_{FB} \times R_A}{V_{OUT} - V_{FB}}$$

where V_{FB} = 0.6V

R_A & R_B value must be rounded to closest standard value

$$C_A = 15\text{pF},\ R_C = 10k\Omega$$

The output voltage should be sensed close to the most distant capacitor from the local output decoupling. All components from the compensation network must be placed as close as possible to the EN6382QI, and the output-voltage-feedback, low-impedance trace should go directly to the controller, keeping the high impedance VFB trace as short as possible.

In order to keep the feedback signal as clean as possible, it is recommended to connect R_B directly to the AGND pin, rather than going through the GND plane.

Compensation and Transient Response

The EN6382QI uses an enhanced type III voltage mode control architecture. Most of the compensation is internal, which simplifies the design. In some applications, improved transient performance may be desired with additional output capacitors (C_{OUT2}). In such an instance, the phase-lead capacitor (C_A) can be adjusted depending on the total output capacitance. Depending on the compensation values , if we adding C_{OUT2} , then the C_A should also be increased. The relationship is linearly shown below:

Table 1: Recommended C_A Capacitor with Adding C_{OUT2}

C_{OUT2}	C_A
100µF	15pF
2~3x100µF	22pF
4~5x100µF	27pF
6~7x100µF	33pF
8x100µF	47pF

As C_{OUT2} increases and the C_A value is adjusted, the device bandwidth will reach its optimization level (at around 1/10th of the switching frequency). Further adjustments by increasing C_{OUT2} and increasing C_A may not yield better transient response or in some situations cause lower gain and phase margin. Over compensating with excessive output capacitance may also cause the device to trigger current limit on startup due to the energy required to charge the output up to regulation level.

Due to such limitations, the recommended maximum output capacitance (C_{OUT2_MAX}) is 800µF and the recommended maximum phase-lead capacitance (C_{A_MAX}) is 47pF.

Input Capacitor Selection

The EN6382QI has been optimized for use with two 1206 22µF input capacitors. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations **must not** be used, as these significantly lose capacitance over frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors may be needed in parallel with the larger capacitors in order to provide high frequency decoupling. The capacitors shown in the Table 2 are typical input capacitors. Other capacitors with similar characteristics may also be used.

Table 2: Recommended Input Capacitors

Description	MFG	P/N
22µF, 10V, 20%, X5R, 1206 (2 capacitors needed)	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T

Output Capacitor Selection

The EN6382QI has been optimized for use with two 1206 47µF output capacitors. Low ESR, X5R or X7R ceramic capacitors are recommended as the primary choice. Y5V or equivalent dielectric formulations **must not** be used as these significantly lose capacitance over frequency, temperature and bias voltage. The capacitors shown in the Recommended Output Capacitors Table 3 are typical output capacitors. Other capacitors with similar characteristics may also be used. Additional bulk capacitance from 100µF to 800µF may be placed beyond the voltage sensing point outside the control loop. This additional capacitance should have a minimum 6mΩ ESR to ensure stable operation. Most tantalum capacitors will have more than 6mΩ of ESR and may be used without special care. Adding distance in layout may help increase the ESR between the feedback sense point and the bulk capacitors.

Table 3: Recommended Output Capacitors

Description	MFG	P/N
47µF, 10V, 20%, X5R, 1206 (2 capacitors needed)	Taiyo Yuden	LMK316BJ476ML-T
47µF, 6.3V, 20%, X5R, 1206 (2 capacitors needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T
10µF, 6.3V, 10%, X7R, 0805 (Optional 1 capacitor in parallel with 2x47µF)	Murata	GRM21BR70J106KE76L
	Taiyo Yuden	JMK212B7106KG-T

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. Placing multiple capacitors in parallel reduces the impedance and hence will result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Table 4: Typical Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p)
2 x 47 µF	<10mV

† 20 MHz bandwidth limit measured on Evaluation Board

THERMAL CONSIDERATIONS

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EN6382QI DC-DC converter is packaged in a 8x8x3mm 56-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The EN6382QI is guaranteed to support the full 8A output current up to 105°C ambient temperature. The following example and calculations illustrate the thermal performance of the EN6382QI.

Example:

V_{IN} = 5.5V

V_{OUT} = 3.3V

I_{OUT} = 8A

First calculate the output power.

P_{OUT} = 1V x 6A = 26.4W

Next, determine the input power based on the efficiency (η) shown in Figure 6.

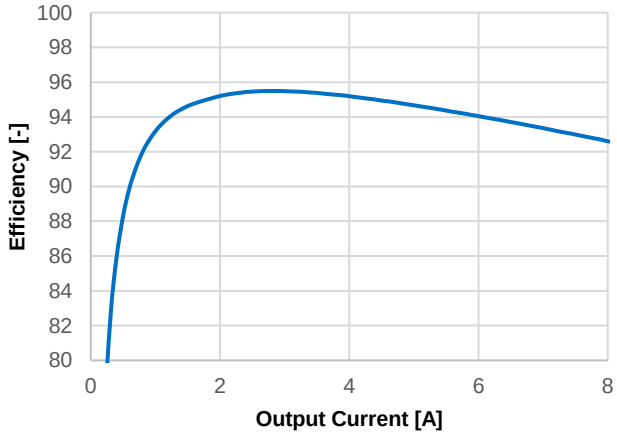


Figure 6: Efficiency V_{IN} =5.5V, V_{OUT} = 3.3V

For V_{IN} = 5.5V, V_{OUT} = 3.3V at 8A, η ≈ 92.5%

η = P_{OUT} / P_{IN} = 92.5% = 0.925

P_{IN} = P_{OUT} / η

P_{IN} ≈ 26.4W/ 0.925 ≈ 28.54W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 28.54W – 26.4W ≈ 2.14W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta J_A value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN6382QI has a θ_{JA} value of 16 °C /W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 2.14W x 16°C/W = 34.2°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 34.2°C ≈ 59.2°C

With 2.14W dissipated into the device, the T_J will be 59.2°C.

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 34.2°C ≈ 90.8°C

The ambient temperature can actually rise to 90°C before the device will reach T_{JMAX}. This indicates that the EN6382QI can support the full 8A output current range up to approximately 90°C ambient temperature given the input and output voltage conditions. This allows the EN6382QI to guarantee full 8A output current capability at 90°C with room for margin. Note that the efficiency will be slightly lower at higher temperatures and this estimate will be slightly lower.

APPLICATION CIRCUITS

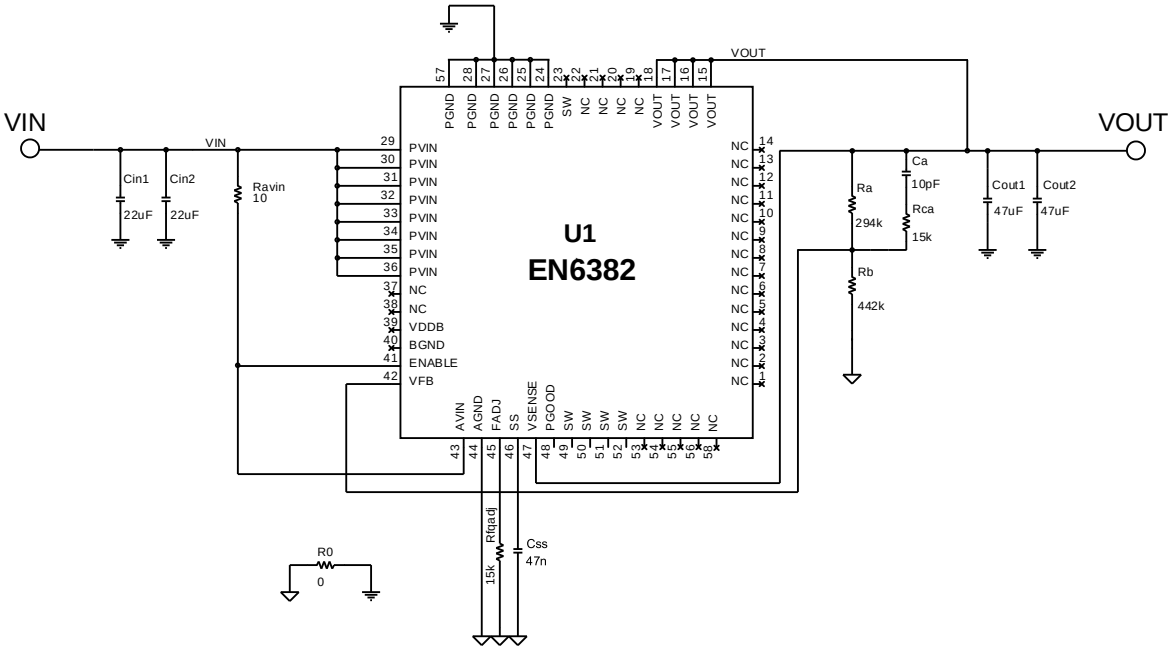


Figure 7: Engineering Schematic with Engineering Notes

LAYOUT RECOMMENDATIONS

This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode with ENABLE tied to AVIN. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files on EN6382QI's product page at https://www.intel.com/content/www/us/en/power/programmable/devices.html#powersoc-converters for details on all layers.

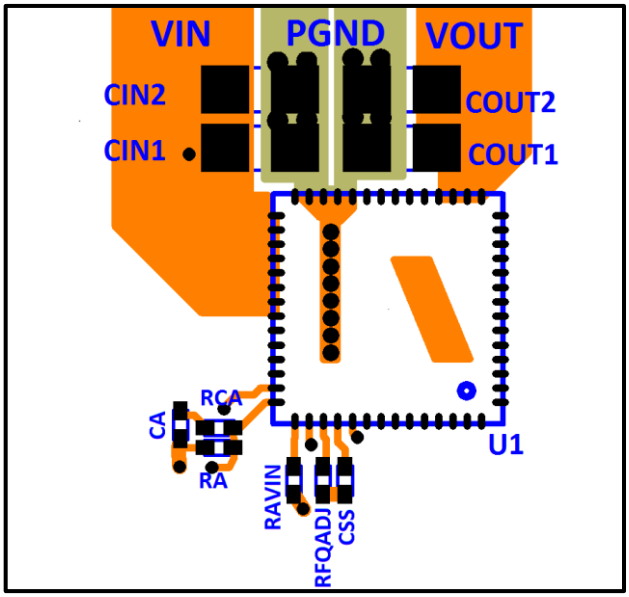


Figure 8: Top Layout with Critical Components Only (Top View).

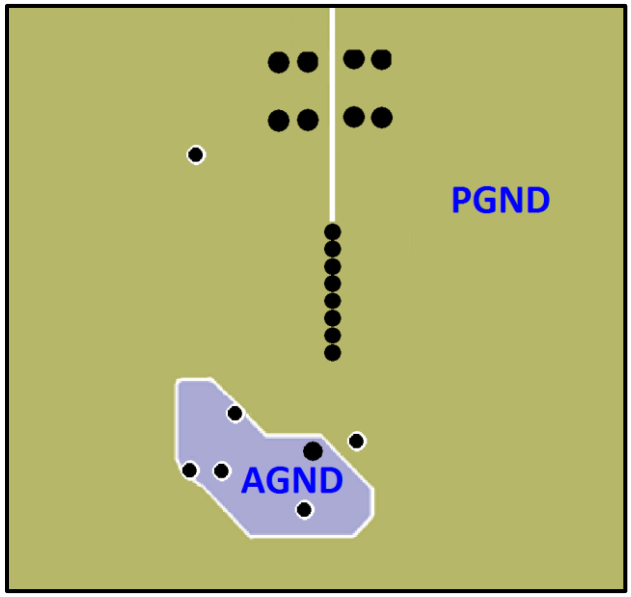


Figure 9: Inner Layer 2 – grounds

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN6382QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN6382QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops. The "x" marks indicate plane connecting VIAs.

Recommendation 3: Using copper planes greatly reduces grounds parasitic inductance and improves decoupling. Same PGND slit can be noticed on this layer as on all the rest. This is not compulsory but it is recommended when possible.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many VIAs as possible. The drill diameter of the VIAs should be 0.33mm, and the VIAs must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the VIAs to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small VIAs (the same size as the thermal VIAs discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these VIAs along the edge of the GND copper closest to the +V copper. These VIAs

connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

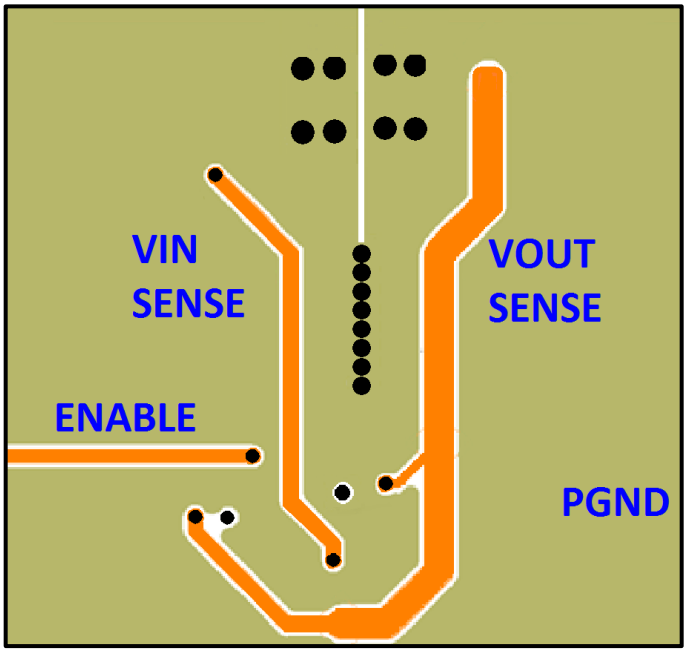


Figure 10: Inner Layer 3 – routing

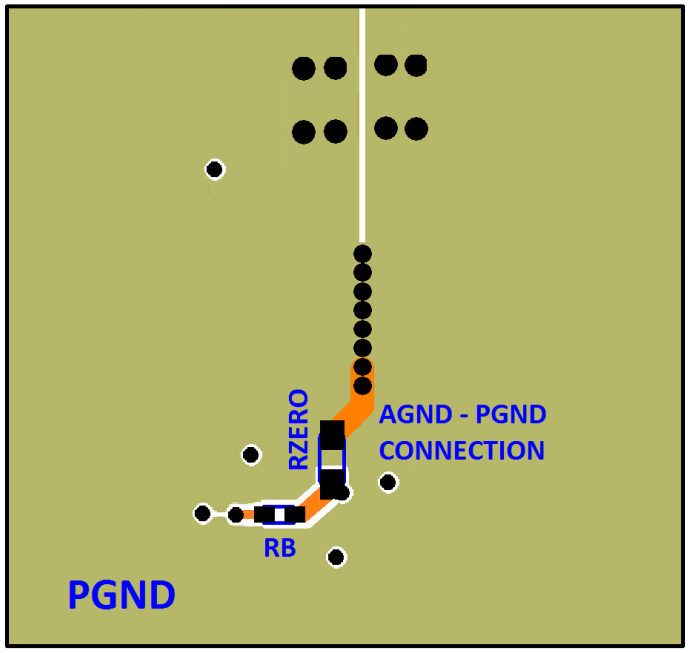


Figure 11: Bottom Layer – components

Recommendation 6: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 8. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: Using separate nets for AGND and PGND is good practice, allowing a proper layout. This is not absolutely necessary but highly recommended (Figure 11).

Recommendation 9: The input and output sense points should be just after the last filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 10: Keep R_A, C_A, R_B, and R_C close to the VFB pin (Refer to Figure 5). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible.

Recommendation 11: Follow all the layout recommendations as close as possible to optimize performance. Enpirion Intel provides schematic and layout reviews for all customer designs. Please contact local Sales Representatives for references to Power Applications support.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 12.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN6382QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 13 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad and mechanical pad. This will prevent excess solder causing bridging between adjacent pins or other exposed metal under the package. Figure 14 shows the recommended solder stencil drawing. Please consult(https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/enpirion_soldering_guidelines.pdf) Soldering Guidelines for more details and recommendations.

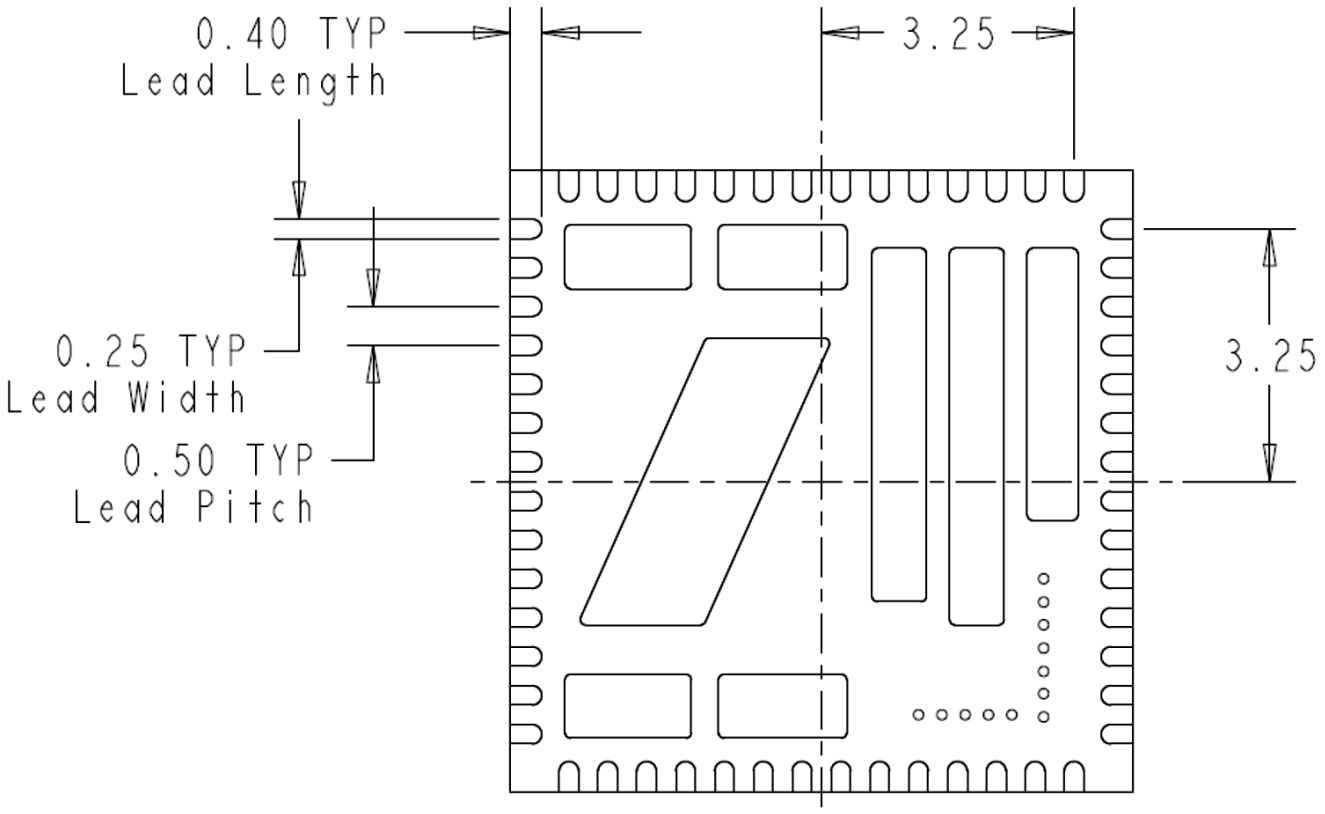


Figure 12: Lead-Frame exposed metal (Bottom View)

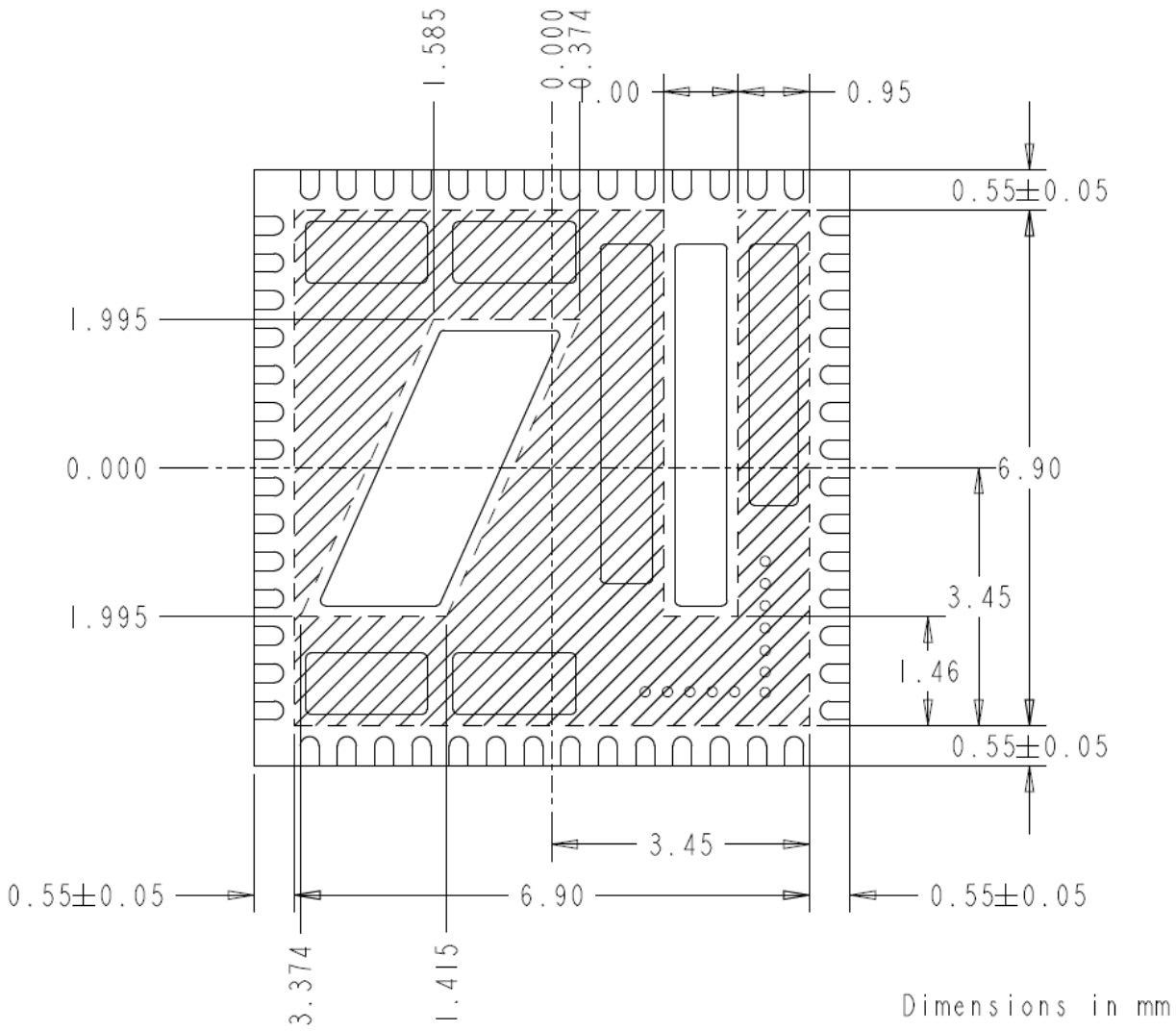


Figure 13: EN6382QI Package – PCB Footprint Keepout (Bottom view)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

PCB FOOTPRINT GUIDE

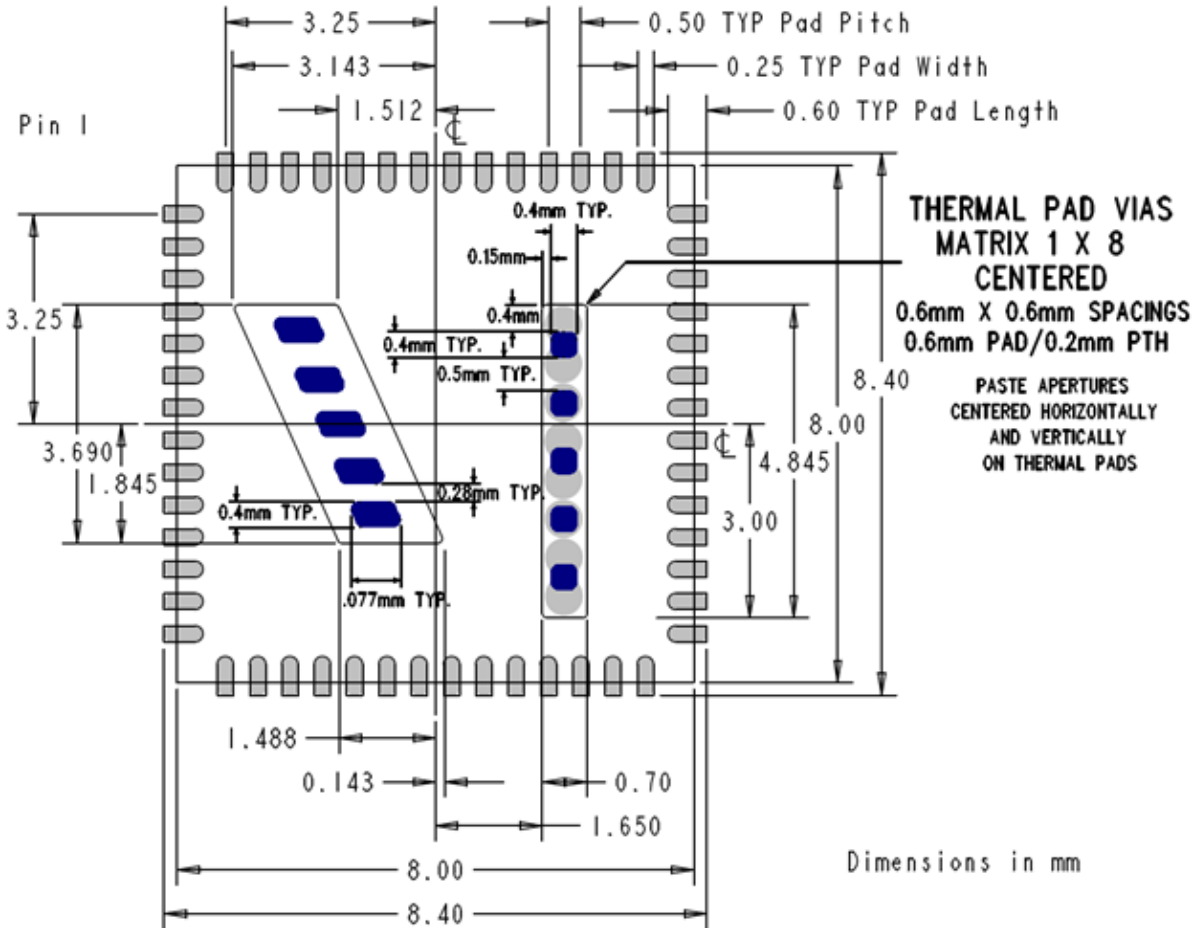


Figure 14: EN6382QI PCB Footprint (Top View)

The solder stencil aperture for the non-perimeter pads is shown in blue in Figure 14 and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

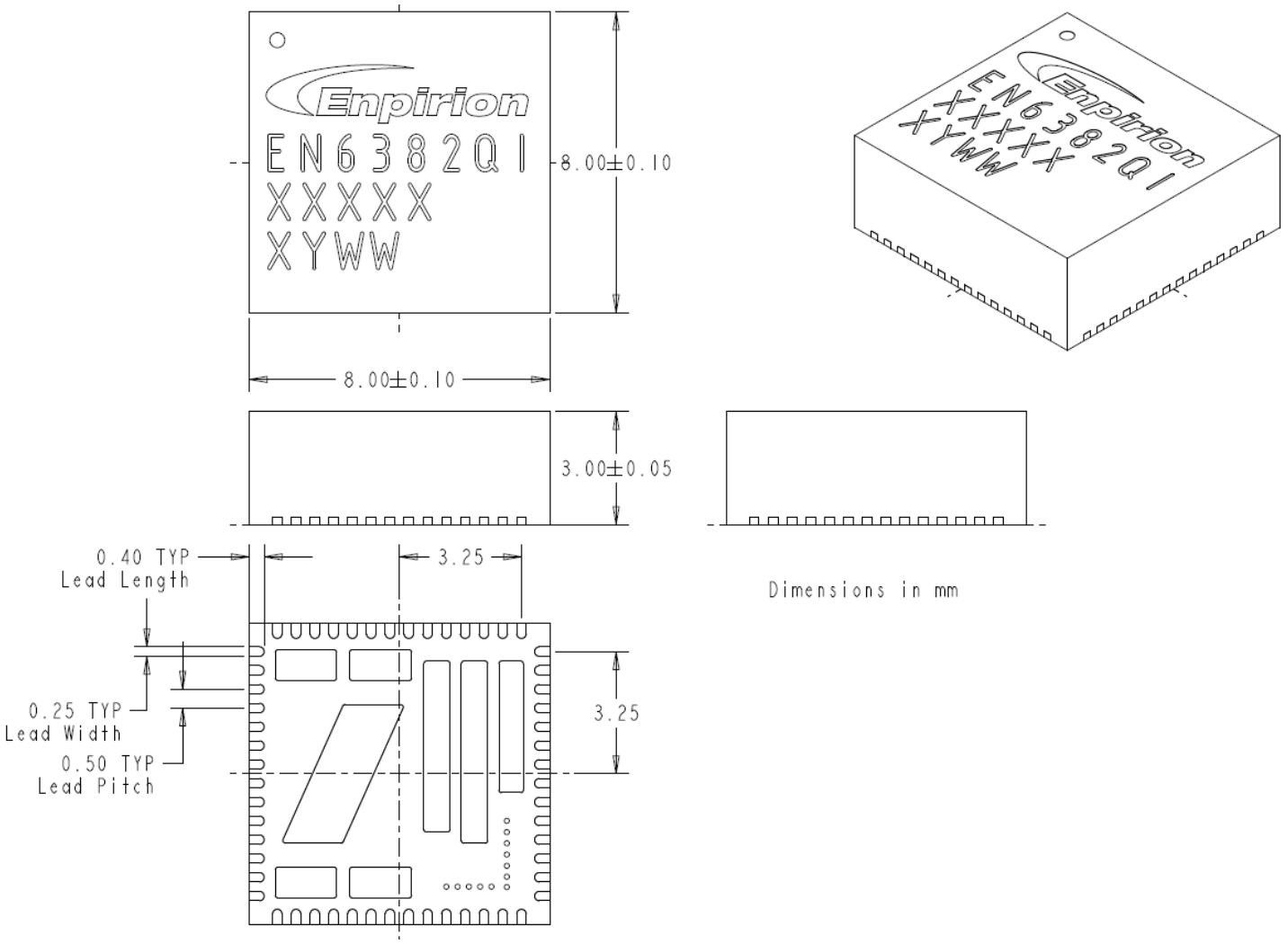


Figure 15: EN6382QI Package Dimensions

Packing and Marking Information: https://www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
A	Feb 2017	Introductory production datasheet
B	Oct 2018	Changed datasheet into Intel format Added Compensation and Transient Response

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

http://www.intel.com/enpirion