PCN Number:	20190219000.0	PCN Date:	February 19, 2019
Title:	Datasheet for TPS65916		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

TPS65916

SLVSD09C – MARCH 2016 – REVISED FEBRUARY 2019

Changes from Revision B (March 2017) to Revision C **Page**

- Added footnote recommending not to pull open-drain GPIOs up to an always-on voltage domain 9
- Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See *Electrical Characteristics: LDO Regulators* for more information. 12
- Added LDO and SMPS output capacitance footnote 13
- Added SMPS Output voltage slew rate description 15
- Changed the comparison condition from VCCA to VCC_SENSE in the *Embedded Power Controller* section 32
- Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence. 33
- Changed discharge resistance to match electrical characteristics table 42
- Changed description of clock dithering from internal to external only 44
- Added information about shutdown timing during short circuit detection 45
- Updated POWERGOOD block diagram and description to clarify dual phase operation. 46
- Added notes to the *SMPS Controls for DVS* image 48
- Added the equation to convert GPADC code to internal die temperature in the *12-Bit Sigma-Delta General-Purpose ADC (GPADC)* section 52
- Additional description of VSYS_LO functionality 66
- Added details on identifying device version. 69
- SMPS and LDO output capacitance specification further explained 74
- Added design considerations for VCCA capacitance to support loss of power 74
- Corrected 9-Vpp with 7V absolute maximum specification in the *Layout Guidelines* section 79
- Updated requirements relating to measurement of high-side and low-side FETs in the *Layout Guidelines* section 80
- Updated images and description on differential measurements across high-side and low-side FETs 81

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS65916	SLVSD09B	SLVSD09C

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/TPS65916

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

TPS659161RGZR	TPS659162RGZR	TPS659162RGZT	TPS659163RGZR
TPS659163RGZT			

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
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