Product Change Notice (PCN)

Subject: Datasheet change for the listed TW8836* Intersil Products
Publication Date: 4/21/2015
Effective Date: 7/21/2015

Revision Description:
Initial Release

Description of Change:
Datasheet change regarding the Serial bus interface (table 10). Changed maximum value for MC_SCLK Clock Frequency from 300 to 400.

Reason for Change:
The change aligns the data sheet with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the change are contained on the following page.

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts.

Qualification status: Complete, see attached
Sample availability: 4/21/2015
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

Appendix A – Affected Products List
Appendix B – Datasheet update

Appendix A – Affected Products List

TW8836AT-LB2-GE	TW8836AT-LB2-GET	TW8836-BB2-CR
TW8836AT-LB2-GER5303	TW8836AT-LB2GETR5303	TW8836-LB2-CE

Appendix B – Datasheet update

From:

TABLE 6. SERIAL BUS INTERFACE TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Bus Free Time between STOP and START	t_{BF}	740	-	-	ns
MC_SDA setup time	t_{sSDAT}	74	-	-	ns
MC_SDA hold time	t_{hSDAT}	50	-	-	ns
Setup time for START condition	t_{sSTA}	370	-	-	ns
Setup time for STOP condition	t_{sSTOP}	370	-	-	ns
Hold time for START condition	t_{hSTA}	74	-	-	ns
Rise time for MC_SCLK and MC_SDA	t_R	-	-	300	ns

To:

TABLE 10. SERIAL BUS INTERFACE TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Bus Free Time between STOP and START	t_{BF}	740	-	-	ns
MC_SDA Setup Time	t_{sSDAT}	74	-	-	ns
MC_SDA Hold Time	t_{hSDAT}	50	-	-	ns
Setup Time for START Condition	t_{sSTA}	370	-	-	ns
Setup Time for STOP Condition	t_{sSTOP}	370	-	-	ns
Hold Time for START Condition	t_{hSTA}	74	-	-	ns
Rise Time for MC_SCLK and MC_SDA	t_R	-	-	300	ns
Fall Time for MC_SCLK and MC_SDA	t_F	-	-	300	ns
Capacitive Load for Each Bus Line	Cbus	-	-	400	pF
MC_SCLK Clock Frequency	f_{sclk}	-	-	400	kHz