# W83601G

# Nuvoton GPI/O Expander

2009/Mar.  Ver. 1.31

## *Table of Contents-*

## 1. GENERAL DESCRIPTION

The W83601G are general purpose input/output ICs with SMBus™( $I^2C$ ). The W83601G provides 15 GPI/O pins. The W83601G provides SMBus™ ($I^2C$) address setting pins to set the address during power- on reset or from external reset.

SMBus™ Address of the W83601G is:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |

The W83601G also provides an interrupt to inform the system that a transition occurs on General Purpose (GP) input pins.

## 2. FEATURES

- SMBus compliance with 3.3V voltage levels
- Two GPI/O ports which provides more flexibility
- Issue interrupts to notify the system that an event occurs
- GP output can be level or pulse mode
- Interrupt output can be in the level or pulse mode
- Internal power-on reset or external RST# pin reset
- Programmable POWER LED output

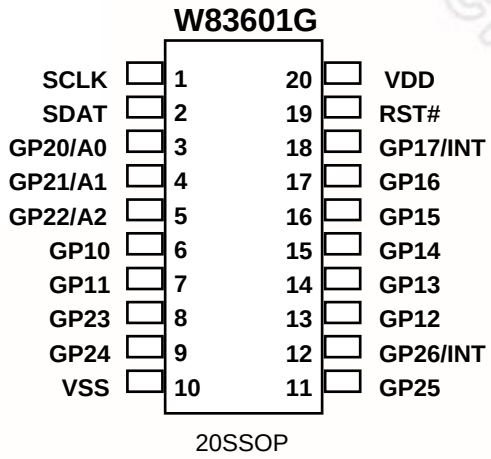
## 3. PACKAGE

- The W83601G is 20-pin SSOP Pb-free (RoHS compatible) package.

## 4. KEY SPECIFICATIONS

- Supply Voltage 5V
- Operating Supply Current 1 mA typ.
- Operating Temperature 0 - 70 °C

## 5. PIN CONFIGURATION




20SSOP

## 6. PIN DESCRIPTION

| | |
|---|---|
| $I/OD_{24t}$ | - TTL level bi-directional pin open drain output with 24 mA sink capability |
| $I/OD_{12ts}$ | - TTL level bi-directional pin open drain output with 12 mA sink capability and schmitt-trigger level input |
| $I/O_{21}$ | - CMOS level bi-directional pin with 21 mA source-sink capability |
| $IN_t$ | - TTL level input pin |
| $IN_{cd}$ | - CMOS level input pin with internal pull down resistor |
| $IN_{ts}$ | - TTL level Schmitt-trigger input pin |
| $OD_{24}$ | - Open drain output pin with 24 mA sink capability |

## 6.1 W83601G Universal General Purpose I/O Port for I²C BUS

| PIN | SYMBOL | I/O | FUNCTION |
|---|---|---|---|
| 1 | SCL | $IN_{ts}$ | SMBus Clock. ($I^2C$ clock) |
| 2 | SDA | $I/OD_{12ts}$ | SMBus bi-directional Data.($I^2C$ data) |
| 3 | GP20<br>A0 | $I/O_{21}$<br>$IN_{cd}$ | General Purpose I/O. **This pin is a setting pin for SMBus ($I^2C$) address bit 0 during power-on reset or RST# pin reset.** |
| 4 | GP21<br>A1 | $I/O_{21}$<br>$IN_{cd}$ | General Purpose I/O. **This pin is a setting pin for SMBus ($I^2C$) address bit 1 during power-on reset or RST# pin reset.** |
| 5 | GP22<br>A2 | $I/O_{21}$<br>$IN_{cd}$ | General Purpose I/O. **This pin is a setting pin for SMBus ($I^2C$) address bit 2 during power-on reset or RST# pin reset.** |
| 6 | GP10 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 7 | GP11 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 8 | GP23 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 9 | GP24 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 10 | VSS | PWR | Ground Pin. |
| 11 | GP25 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 12 | GP26<br>INT | $I/OD_{24t}$<br>$OD_{24}$ | General Purpose I/O default input.<br>Auto-generate Interrupt signal when a transition on GPI inputs is detected. This interrupt is either on pin12 or pin18. |
| 13 | GP12 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 14 | GP13 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 15 | GP14 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 16 | GP15 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 17 | GP16 | $I/OD_{24t}$ | General Purpose I/O default input. |
| 18 | GP17<br>INT | $I/OD_{24t}$<br>$OD_{24}$ | General Purpose I/O default input.<br>Auto-generate Interrupt signal when a transition on GPI inputs is detected. This interrupt is either on pin12 or pin18 |
| 19 | RST# | $In_{ts}$ | Reset signal input. |
| 20 | VDD | PWR | Power Pin. |

# 7. REGISTERS

## 7.1 BRIED OF REGISTER CONTENTS

| INDEX | R/W | DEFAULT | REGISTERS DESCRIPTION |
|---|---|---|---|
| 00h | R | - | GP Port 1: Input Port Data Register |
| 01h | R/W | 00 | GP Port 1: Output Port Data Register |
| 02h | R/W | f0 | GP Port 1: Polarity Inversion Register |
| 03h | R/W | ff | GP Port 1: Input/Output Configuration Register |
| 04h | R/W | 00 | GP Port 1: Output style control Register. |
| 05h | R | - | GP Port 1: Input Latched Data Register. |
| 06-07h | - | - | Reserved Register |
| 08h | R | - | GP Port 2: Input Port Register |
| 09h | R/W | 00 | GP Port 2: Output Port Register |
| 0Ah | R/W | 70 | GP Port 2: Polarity Inversion Register |
| 0Bh | R/W | 7f | GP Port 2: Input/Output Configuration Register |
| 0Ch | R/W | 00 | GP Port 2: Output style control Register. |
| 0Dh | R | - | GP Port 2: Input Latched Data Register. |
| 0E-0Fh | - | - | Reserved Register |
| 10h | R | 00 | GP Port 1: Interrupt Status Register. |
| 11h | R | 00 | GP Port 2: Interrupt Status Register |
| 12h | R/W | 00 | GP Port 1: Interrupt Enable Register |
| 13h | R/W | 00 | GP Port 2: Interrupt Enable Register |
| 14h | R/W | 00 | Mode Configuration Register |
| 15h | R/W | 00 | Power LED Configuration Register |
| 16-1Fh | - | - | Reserved Register |
| 20h | R | 60 | Chip ID High Byte Register |
| 21h | R | 12 | Chip ID Low Byte Register (W83601G) |

## 7.2 W83601G REGISTER DESCRIPTIONS

**CR00 (GP Port 1: Input port Data Register, Default 0x--, Read Only)**

This register is a data port for input only. It reflects the incoming logic levels of the pins defined as an input mode by CR03. The data will be inverted by CR02.

Bit 7 ~ 0: GP17 ~ GP10 Input Data Port.

**CR01 (GP Port 1: Output port Data Register, Default 0x00, Read/Write)**

This register is a data port for output only. It reflects the outgoing logic levels of the pins defined as an output mode by CR03. This register will reflect the value of output Flip-flop during a read access. The output data style will be inverted or changed by CR02 or CR04.

Bit 7 ~ 0: GP17 ~ GP10 Output Data Port.

**CR02 (GP Port 1: Polarity Inversion Register, Default 0xf0, Read / Write)**

This register enables polarity inversion of pins defined as input or output by CR03.

When set to "1", the incoming/outgoing port value is inverted.

When set to "0", the incoming/outgoing port value is the same as in data register.

Bit 7 ~ 0: GP17 ~ GP10 Polarity Inversion Register.

**CR03 (GP Port 1: Input/Output Configuration Register, Default 0xff, Read / Write)**

This register selects Input or Output mode of pins.

When set to "1", respective GPIO port is programmed as an input port.

When set to "0", respective GPIO port is programmed as an output port.

Bit 7 ~ 0: GP17 ~ GP10 Input/Output Configuration Register.

**CR04 (GP Port 1: Output Style Control Register, Default 0x00, Read / Write)**

This register selects Output style of pins as level or pulse.

When set to "1", respective GPIO port is programmed as a pulse signal.

When set to "0", respective GPIO port is programmed as a level signal.

Bit 7 ~ 0: GP17 ~ GP10 Output Style Control Register.

**CR05 (GP Port 1: Input latched data Register, Default 0x--, Read Only)**

This register will latch Port 1 data while power on or RST# pin low, which is controlled by CR14h bit 0.

Bit 7 ~ 0: GP17 ~ GP10 Input latched data.

**CR06-07 Reserved Register**

**CR08 (GP Port 2: Input port Data Register, Default 0x--, Read Only)**

This register is a data port for input only. It reflects the incoming logic levels of the pins defined as an input mode by CR0B. The data will be inverted by CR0A.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Input Data Port.

**CR09 (GP Port 2: Output port Data Register, Default 0x00, Read / Write)**

This register is a data port for output only. It reflects the outgoing logic levels of the pins defined as an output mode by CR0B. This register will reflect the value of output Flip-flop during a read access. The output data style will be inverted or changed by CR0A or CR0C.

Bit 7: Reserved.

Bit 7 ~ 0: GP26 ~ GP20 Output Data Port.

**CR0A (GP Port 2: Polarity Inversion Register, Default 0x70, Read / Write)**

This register enables polarity inversion of pins defined as input or output by CR0B.

When set to "1", the incoming/outgoing port value is inverted.

When set to "0", the incoming/outgoing port value is the same as in data register.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Polarity Inversion Register.

**CR0B (GP Port 2: Input/Output Configuration Register, Default 0x7f, Read / Write)**

This register selects Input or Output mode of pins.

When set to "1", respective GPIO port is programmed as an input port.

When set to "0", respective GPIO port is programmed as an output port.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Input/Output Configuration Register.

**CR0C (GP Port 2: Output Style Control Register, Default 0x00, Read / Write)**

This register selects Output style of pins as level or pulse.

When set to "1", respective GPIO port is programmed as a pulse signal.

When set to "0", respective GPIO port is programmed as a level signal.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Output Style Control Register.

**CR0D (GP Port 2: Input latched data Register, Default 0x--, Read Only)**

This register will latch Port 2 data while power on or RST# pin low, which is controlled by CR14h bit 1.

Bit 7: Reserved.

Bit 6 ~ 0: GP26 ~ GP20 Input latched data, which bit 2-0 are SMBus address bit A2-A0.

**CR0E-0F Reserved Register**

**CR10 (GP Port1: Interrupt Status Register, Default 0x00, Read Only)**

Bit 7-0: = 1, a transition occurs on pin GP17-GP10.

If the interrupt function of GP17/INT is selected, bit 7 of this register will always be 0.

A read will clear this register.

**CR11 (GP Port2: Interrupt Status Register, Default 0x00, Read Only)**

Bit 7: = Reserved.

Bit 6-0: = 1, a transition occurs on pin GP26-GP20.

If the interrupt function of GP26/INT is selected, bit 6 of this register will always be 0.

A read will clear this register.

**CR12 (GP Port 1: Interrupt Enable Register, Default 0x00, Read / Write)**

Bit 7-0: = 0, disable GP17-GP10 interrupt output when the interrupt function is selected.

**CR13 (GP Port 2: Interrupt Enable Register, Default 0x00, Read / Write)**

Bit 7-5: = Reserved.

Bit 6-0: = 0, disable GP26-GP20 interrupt output when the interrupt function is selected.

**CR14 Mode Configuration Register (Default 0x00, Read / Write)**

Bit 7: = 1, Set GP/INT pin as INT function. 0: Set GP/INT pin as GP function.

Bit 6: = 1, Set INT function of GP26 (pin 12). 0: Set INT function at GP17 (pin 18).

Bit 5: = 1, Set INT output pin as pulse mode. 0: set INT output pin as level mode.

Bit 4: = 1, Set INT output pin polarity is 1 (normal high). 0: set INT output pin polarity to 0 (normal low). This bit is only for the W83601R.

Bit 3: = 1, Port 2 (CR09h-CR0Ch, CR11h, CR13h) registers can be reset to default data by the RST# pin. 0, Port 2 (CR09h-CR0Ch) can not be reset by RST# pin.

Bit 2: = 1, Port 1 (CR01h-CR04h, CR10h, CR12h) registers can be reset to default data by the RST# pin. 0, Port 1 (CR01h-CR04h) can not be reset by RST# pin.

Bit 1: = 1, Port 2 CR0Dh can be latched by the RST# pin not only at the resetting instant but also in the power-on period. 0, Port 2 CR0Dh can be latched only in the power-on period.

Bit 0: = 1, Port 1 CR05h can be latched by the RST# pin not only at the resetting instant but also in the power-on period. 0, Port 1 CR05h can only be latched in the power-on period.

**CR15 Power LED Configuration Register (Default 0x00, Read/Write)**

**Priority of LED function is highest.**

Bit 7: = 1, Enable the LED function. 0, Disable the LED function.

When the LED function is enabled, GP function is ignored, no matter it is input or output.

Bit 6-4: LED frequency selection.

= 111, the LED pin is tri-state (OD pin) or driven high (O pin).

= 110, the LED pin is a 1 Hz toggle pulse with 50 duty cycle.

= 101, the LED pin is a 1/2 Hz toggle pulse with 50 duty cycle.

= 100, the LED pin is a 1/4 Hz toggle pulse with 50 duty cycle.

= 000, the LED pin is driven low.

Bit 3: GP port selection.

0, GP port 1 is set to the LED function if bit 7 is set to 1.

1, GP port 2 is set to the LED function if bit 7 is set to 1.

Bit 2-0: GP pin selection.

=110-000, GP16-GP10 can be selected as LED output when bit 3 is 0.

=101-011, GP25-GP23 can be selected as LED output when bit 3 is 1.

**CR16-1F Reserved Register**

**CR20 (Chip ID High Byte, Read Only)**

Bit 7-0: = 0x60.

**CR21 (Chip ID Low Byte, Read Only)**

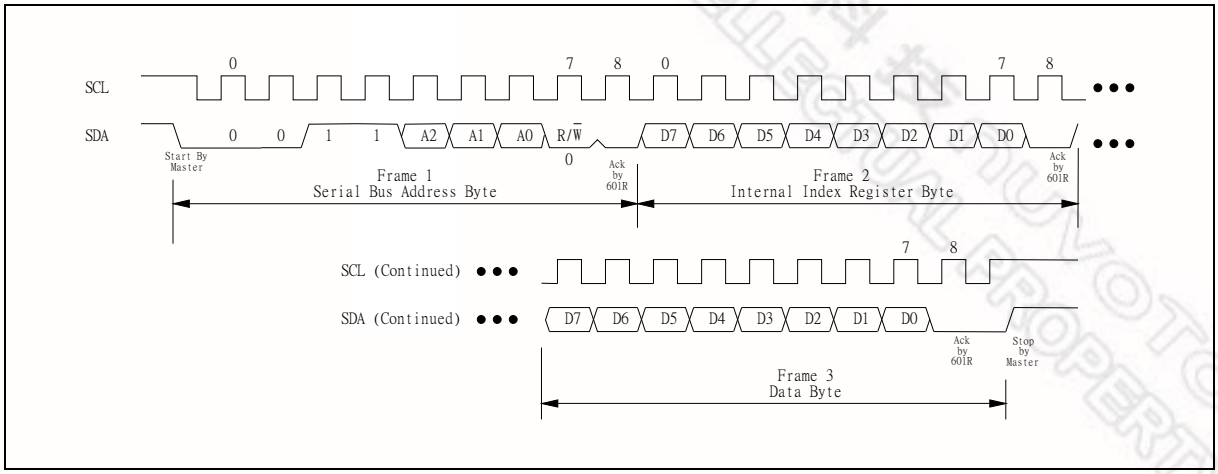
Bit 7-0: = 0x13 (for the W83601G).

# 8. FUNCTION DESCRIPTIONS

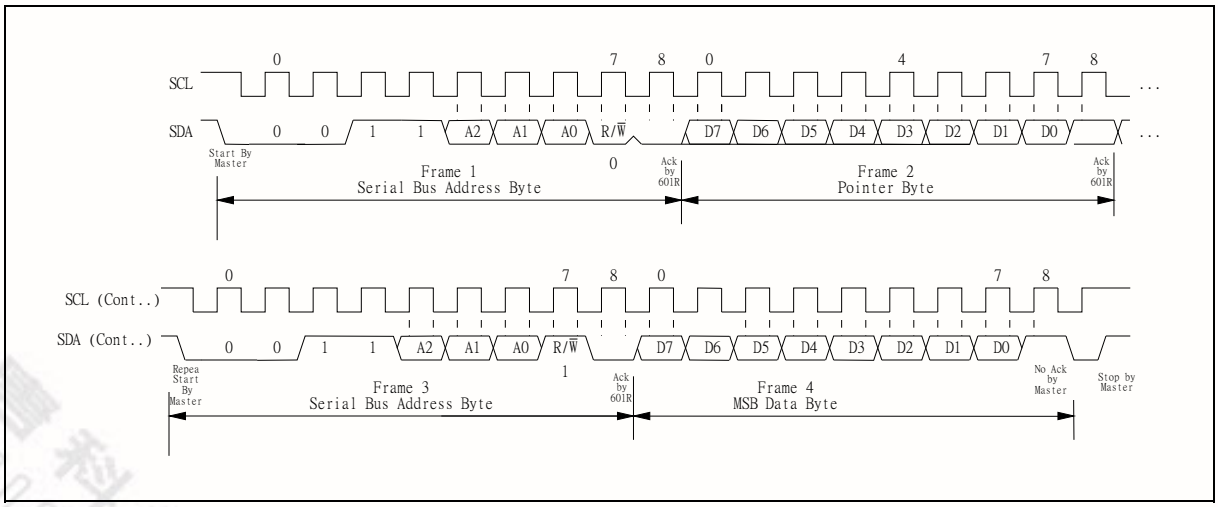
## 8.1 ACCESS INTERFACE

The W83601G provides a two-wired serial interface which is compliant with SMBus™ 1.0 Write Byte and Read Byte protocol.

### 8.1.1 Write a data into the W83601G register




### 8.1.2 Read a data from the W83601G register



## 8.2 GPI/O Output Mode:

### 8.2.1 GPO output

Tow output modes for GPO. One is LEVEL and the other is PULSE.

| GPO OUTPUT STYLE | POLARITY | OUTPUT PORT REGISTER | OUTPUT VALUE AT PIN | WAVE |
|---|---|---|---|---|
| Level | 0 | 0 | 0 | |
| | | 1 | 1 | |
| | 1 | 0 | 1 | |
| | | 1 | 0 | |
| Pulse | 0 | write 1 | Active | |
| | 1 | write 1 | Active | |

### 8.2.2 INT output

There are two output modes for the INT pin. One is the LEVEL mode and the other is PULSE.

| INT OUTPUT MODE | POLARITY | OUTPUT | WAVE |
|---|---|---|---|
| Level | 0(normal low) | 1 | |
| | 1(normal high) | 0 | |
| Pulse | 0(normal low) | High Pulse | |
| | 1(normal high) | Low Pulse | |

In the Level mode, if INT is activated, it will be de-activated when the interrupt status registers are read.

In the Pulse mode, interrupt will be activated again unless all of the enabled interrupt status registers are read.

### 8.2.3 GPI interrupt status

Once a transition occurs on the GPI input pins, the interrupt status registers (CR10, CR11) will be set. At the mean time, if the interrupt function is enabled, the INT pin will generate an interrupt. Reading these interrupt registers will clear themselves and reset the interrupt. If an interrupt occurs but the interrupt status registers are not read, the interrupt will not be generated again.

# 9. DC AND AC SPECIFICATION

## 9.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage | -0.5 to 7.0 | V |
| Input Voltage | -0.5 to $V_{DD}$+0.5 | V |
| Operating Temperature | 0 to +70 | ° C |
| Storage Temperature | -55 to +150 | ° C |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 9.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, $V_{DD}$ = 5V ± 5%, $V_{SS}$ = 0V)

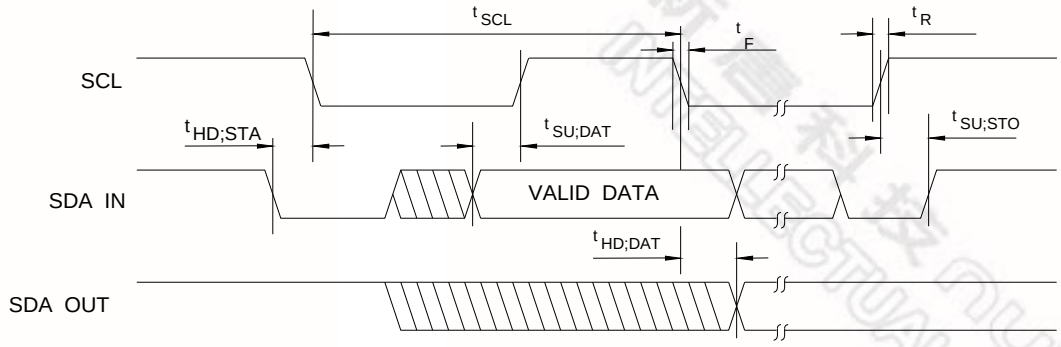
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$I/OD_{12ts}$ - TTL level bi-directional pin open drain with source-sink capability of 12 mA and schmitt-trigger level input** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD}$ = 5 V |
| Hysteresis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$ = 5 V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| | | | | | | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **$IN_t$ - TTL level input pin** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$IN_{ts}$ - TTL level Schmitt-triggered input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD}$ = 5 V |
| Hysteresis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$ = 5 V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |

DC Characteristics, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$IN_{cd}$ - CMOS level input pin with internal pull down** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.3 $V_{DD}$ | V | $V_{DD}$ = 5 V |
| Input High Voltage | $V_{IH}$ | 0.7$V_{DD}$ | | | V | $V_{DD}$ = 5 V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/O_{21}$ - CMOS level bi-direction pin with 21mA source-sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.3 $V_{DD}$ | V | $V_{DD}$ = 5 V |
| Input High Voltage | $V_{IH}$ | 0.7$V_{DD}$ | | | V | $V_{DD}$ = 5 V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 21 mA |
| Output High Voltage | $V_{OH}$ | 3.5 | | | V | $I_{OH}$ = 21 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/OD_{24t}$ - TTL level bi-direction pin open-drain output with 24mA sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$OD_{24}$ - open-drain output pin with 24mA sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |

## 9.3 AC CHARACTERISTICS

### 9.3.1 Serial Bus Timing Diagram

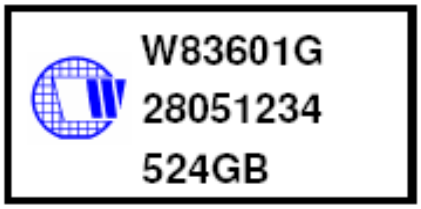



Serial Bus Timing Diagram

**Serial Bus Timing**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| SCL clock period | $t_{SCL}$ | 10 | | uS |
| Start condition hold time | $t_{HD;STA}$ | 4.7 | | uS |
| Stop condition setup-up time | $t_{SU;STO}$ | 4.7 | | uS |
| DATA to SCL setup time | $t_{SU;DAT}$ | 120 | | nS |
| DATA to SCL hold time | $t_{HD;DAT}$ | 5 | | nS |
| SCL and SDA rise time | $t_R$ | | 1.0 | uS |
| SCL and SDA fall time | $t_F$ | | 300 | nS |

## 10. TOP MARKING SPECIFICATION




Left line : chip logo

1st line : Part number : W83601G, Pb-free part.

2nd line : Chip lot no.

3rd line : Tracking code

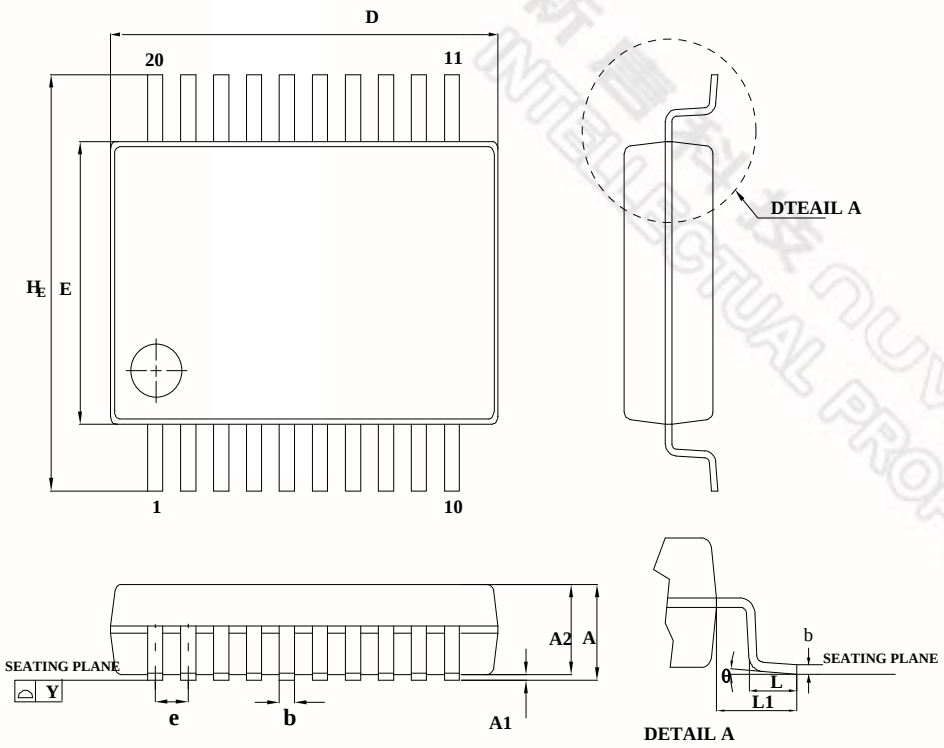
**524** : Package assembled in Year 05', week 24

**G** : Assembly house ID

**B** : the IC version

## 11. PACKAGE DRAWING AND DIMENSIONS

20 SSOP-209 mil




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | — | — | 2.00 | — | — | 0.079 |
| A1 | 0.05 | — | — | 0.002 | — | — |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| b | 0.22 | — | 0.38 | 0.009 | — | 0.015 |
| c | 0.09 | — | 0.25 | 0.004 | — | 0.010 |
| D | 6.90 | 7.20 | 7.50 | 0.272 | 0.283 | 0.295 |
| E | 5.00 | 5.30 | 5.60 | 0.197 | 0.209 | 0.220 |
| $H_E$ | 7.40 | 7.80 | 8.20 | 0.291 | 0.307 | 0.323 |
| e | — | 0.65 | — | — | 0.0256 | — |
| L | 0.55 | 0.75 | 0.95 | 0.021 | 0.030 | 0.037 |
| L1 | — | 1.25 | — | — | 0.050 | — |
| Y | — | — | 0.10 | — | — | 0.004 |
| θ | 0 | — | 8 | 0 | — | 8 |

## 12. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| | | n.a. | All the version before 0.30 are for internal use. |
| 0.3 | 99/08 | n.a. | First publication. |
| 0.31 | 99/08 | P.4,5<br>P.6<br>P.10<br>P.13 | Change Pin Description of W83601R pin 3,4,5.<br>Change Pin Description of W83602R pin 3,4.<br>Update Register Table.<br>CR16 is a reserved register. Please ignore it.<br>Change INT output description. |
| 0.32 | 99/09 | P.10 | CR15 bit 3 description. |
| 0.33 | 01/02 | P.11 | Insert 8.1 section – Access interface |
| 0.34 | 01/02 | P.10 | Update CR21 Chip ID. |
| 0.35 | 01/03 | P.4 | Update pin characteristic.<br>Update application schematic to version 0.3. |
| 0.4 | 01/06 | P.15 | Add chapter 9 DC and AC specification. |
| 0.5 | 01/08 | P.15 | Update chapter 9.2 DC specification |
| 0.6 | 05/04 | n.a. | Add Pb-free package |
| 1.0 | 05/26 | P.20 | ADD Important Notice |
| 1.1 | 05/12 | P.3; P.18~19 | Add Pb-free package description, and top marking description. |
| 1.2 | 07/11 | | Remove the W83602R/G, it's not recommend for new design. |
| 1.3 | 2008/July | | Change logo<br>Remove the leaded part number W83601R |
| 1.31 | 2009/Mar. | | Correct the typo in the package dimension |

## Important Notice

**Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instructments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.**

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