SN65HVD888 Bus-Polarity Correcting RS-485 Transceiver With IEC-ESD Protection

1 Features

- Exceeds Requirements of EIA-485 Standard
- Bus-Polarity Correction Within 76 ms (t_{FS})
- Data Rate: 300 bps to 250 kbps
- Works With Two Configurations:
  - Failsafe Resistors Only
  - Failsafe and Differential Termination Resistors
- Up to 256 Nodes on a Bus (1/8 Unit Load)
- SOIC-8 Package for Backward Compatibility
- Bus-Pin Protection:
  - ±16 kV HBM protection
  - ±12 kV IEC61000-4-2 Contact Discharge
  - +4 kV IEC61000-4-4 Fast Transient Burst

2 Applications

- E-Metering Networks
- Industrial Automation
- HVAC Systems
- DMX512-Networks
- Process Control
- Battery-Powered Applications
- Motion Control
- Telecom Equipment

3 Description

The SN65HVD888 is a low-power RS-485 transceiver with automatic bus-polarity correction and transient protection. Upon hot plug-in, the device detects and corrects the bus polarity within the first 76 ms of bus idling. On-chip transient protection protects the device against IEC61000 ESD and EFT transients. This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to electrostatic discharge (ESD) events, with high levels of protection to Human-Body Model (HBM), Air-Gap Discharge, and Contact Discharge specifications.

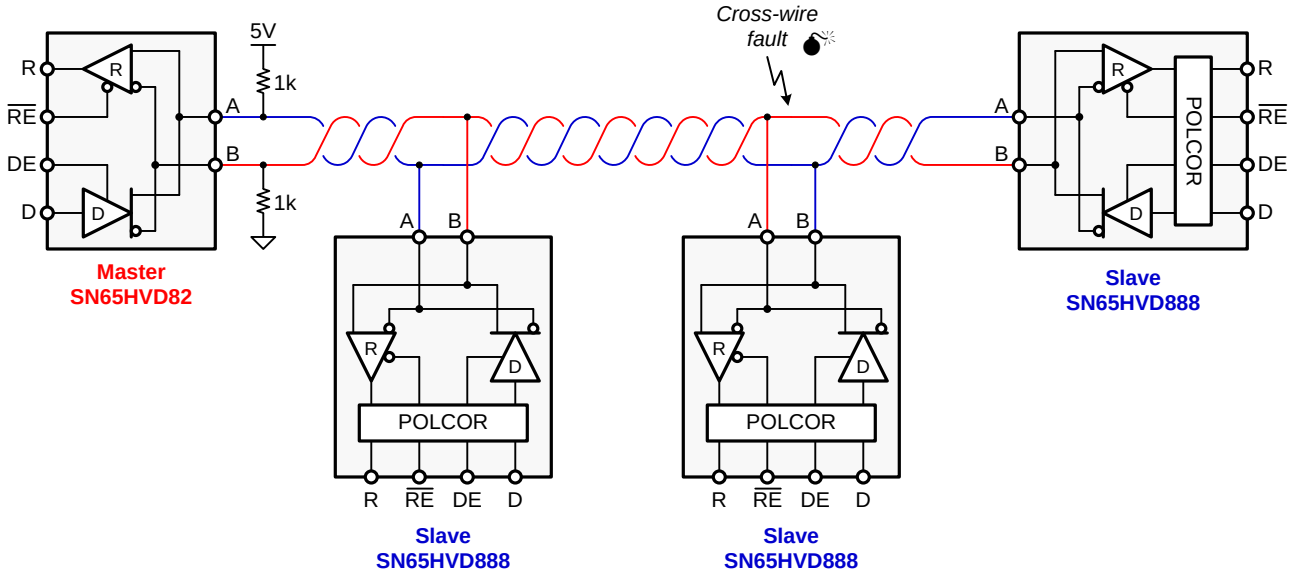
The device combines a differential driver and a differential receiver, which operate together from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The SN65HVD888 is available in an SOIC-8 package, and is characterized from –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD888	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Network Application With Polarity Correction (POLCOR)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2017) to Revision C — **Page**

- Changed 3.3 V_{ISO} To: 5 V_{ISO} in Figure 24 ... 20

Changes from Revision A (September 2015) to Revision B — **Page**

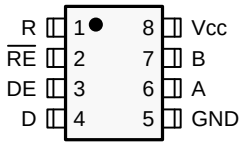
- Changed text From: "characterized from –40°C to 85°C" To: "characterized from –40°C to 125°C" in the *Description* ... 1
- Changed the T_A MAX value From: 85°C To: 125°C in the *Recommended Operating Conditions* table ... 4
- Changed I_{CC} to show values for the temperature ranges of –40°C to 85°C and –40°C to 125°C in the *Electrical Characteristics* table ... 5

Changes from Original (July 2013) to Revision A — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed JEDEC Standard 22, Test Method A114 (HBM) from ±4 to ±8 kV. ... 3
- Changed JEDEC Standard 22, Test Method A115 (Machine Model) from ±100 to ±200 V. ... 3
- Changed the "D and $\overline{RE}$ Inputs" circuit and the "DE Input" circuit of Figure 15 ... 13

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

(see (1))

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
	Input voltage at any logic pin	–0.3	5.7	V
	Voltage input, transient pulse, A and B, through 100 Ω	–100	100	V
	Voltage at A or B inputs	–18	18	V
	Receiver output current	–24	24	mA
	Continuous total-power dissipation	See (*Thermal Information*) table		
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings: JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±12000	V
		IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND	±4000	
		IEC 60749-26 ESD (HBM), bus terminals and GND	±16000	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ID}	Differential input voltage		–12		12	V
V_I	Input voltage at any bus terminal (separate or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver-enable, and receiver-enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
C_L	Differential load capacitance			50		pF
R_L	Differential load resistance			60		Ω
$1/t_{UI}$	Signaling rate		0.3		250	kbps
T_J	Junction temperature		–40		150	°C
T_A(2)	Operating free-air temperature (see *Thermal Information* for additional information)		–40		125	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

6.5 Thermal Information

THERMAL METRIC(1)		SN65HVD888 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Driver differential-output voltage magnitude	RL = 60 Ω, 375 Ω on each output from –7 to +12 V	See Figure 4	1.5	2.5		V
		RL = 54 Ω (RS-485)	See Figure 5	1.5	2.5		
		RL = 100 Ω (RS-422)		2	3		
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of driver differential-output voltage	RL = 54 Ω, CL = 50 pF	See Figure 5	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors	See Figure 5	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage	Center of two 27-Ω load resistors	See Figure 5	–0.2	0	0.2	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors	See Figure 5		850		mV
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential-input voltage threshold				35	100	mV
$V_{IT–}$	Negative-going receiver differential-input voltage threshold			–100	–35		mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA
I_{OZ}	Receiver high-impedance output current	VO = 0 V or VCC, $\overline{RE}$ at V_{CC}		–10		10	µA
$\lvert I_{OS} \rvert$	Driver short-circuit output current	$\lvert I_{OS} \rvert$ with V_A or V_B from –7 to +12 V				150	mA
I_I	Bus input current (driver disabled)	V_{CC} = 4.5 to 5.5 V or	V_I = 12 V		75	125	µA
		V_{CC} = 0 V, DE at 0 V	V_I = –7 V	–100	–40		
I_{CC}	Supply current (quiescent) –40°C to 85°C	Driver and receiver enabled	$\overline{DE}$ = V_{CC}, $\overline{RE}$ = GND, No load		750	900	µA
		Driver enabled, receiver disabled	$\overline{DE}$ = V_{CC}, $\overline{RE}$ = V_{CC}, No load			650	
		Driver disabled, receiver enabled	$\overline{DE}$ = GND, $\overline{RE}$ = GND, No load			750	
		Driver and receiver disabled	DE = GND, $\overline{D}$ = GND $\overline{RE}$ = VCC, No load		0.4	5	
I_{CC}	Supply current (quiescent) –40°C to 125°C	Driver and receiver enabled	$\overline{DE}$ = V_{CC}, $\overline{RE}$ = GND, No load		750	990	µA
		Driver enabled, receiver disabled	$\overline{DE}$ = V_{CC}, $\overline{RE}$ = V_{CC}, No load			715	
		Driver disabled, receiver enabled	$\overline{DE}$ = GND, $\overline{RE}$ = GND, No load			825	
	Supply current (dynamic)	See Figure 3					

(1) Under any specific conditions, V_{IT+} is specified to be at least V_{HYS} higher than $V_{IT–}$.

6.7 Power Dissipation Characteristics

PARAMETER			TEST CONDITIONS	VALUE	UNIT
PD	Power Dissipation driver and receiver enabled, V_{CC} = 5.5 V, T_J = 150°C 50% duty cycle square-wave signal at 250 kbps signaling rate:	Unterminated	R_L = 300 Ω, C_L = 50 pF (driver)	164	mW
		RS-422 load	R_L = 100 Ω, C_L = 50 pF (driver)	247	
		RS-485 load	R_L = 54 Ω, C_L = 50 pF (driver)	316	

6.8 Switching Characteristics

3.3 ms > bit time > 4 µs (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential-output rise and fall times	RL = 54 Ω, CL = 50 pF	See Figure 6	400	700	1200	ns
t_{PHL}, t_{PLH}	Driver propagation delay	RL = 54 Ω, CL = 50 pF	See Figure 6	90	700	1000	ns
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	RL = 54 Ω, CL = 50 pF	See Figure 6		25	200	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 7 and Figure 8		50	500	ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled	See Figure 7 and Figure 8		500	1000	ns
		Receiver disabled	See Figure 7 and Figure 8		3	9	µs
RECEIVER							
t_r, t_f	Receiver output rise and fall times	CL = 15 pF	See Figure 9		18	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	CL = 15 pF	See Figure 9		85	195	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	CL = 15 pF	See Figure 9		1	15	ns
t_{PHZ}, t_{PLZ}	Receiver disable time				50	500	
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 10		20	130	ns
		Driver disabled	See Figure 11		2	8	µs
t_{FS}	Bus failsafe time	Driver disabled	See Figure 12	44	58	76	ms

6.9 Typical Characteristics

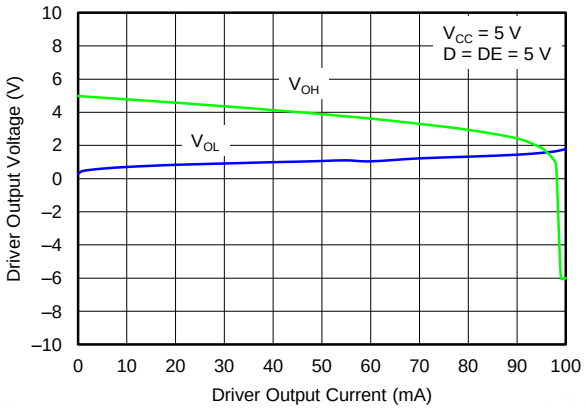


Figure 1. Driver Output Voltage vs Driver Output Current

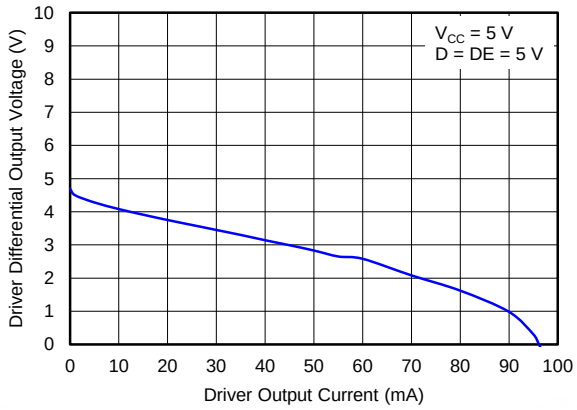


Figure 2. Driver Differential Output Voltage vs Driver Output Current

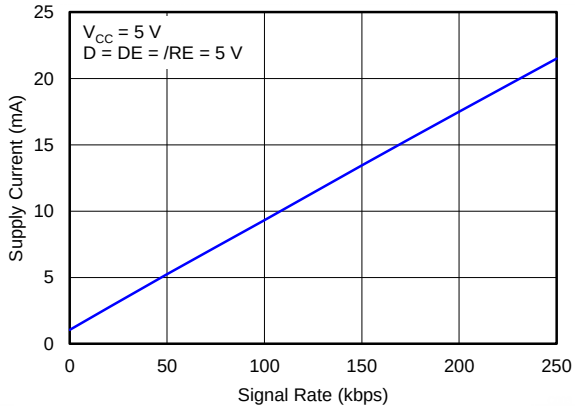


Figure 3. Supply Current vs Signaling Rate

7 Parameter Measurement information

7.1 Driver

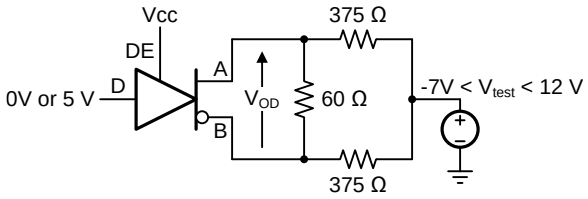


Figure 4. Measurement of Driver Differential-Output Voltage With Common-Mode Load

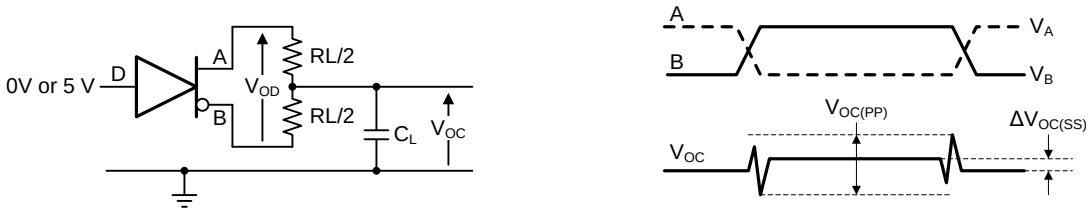


Figure 5. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

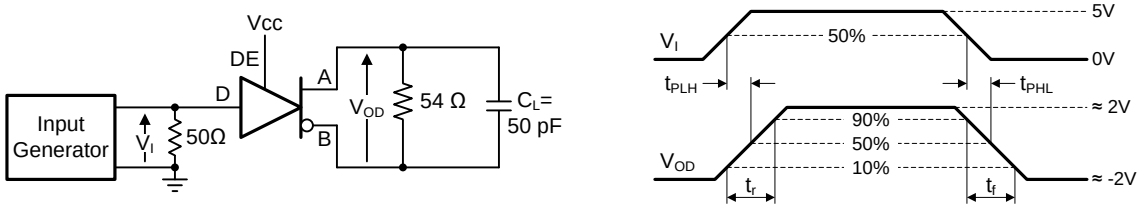


Figure 6. Measurement of Driver Differential-Output Rise and Fall Times and Propagation Delays

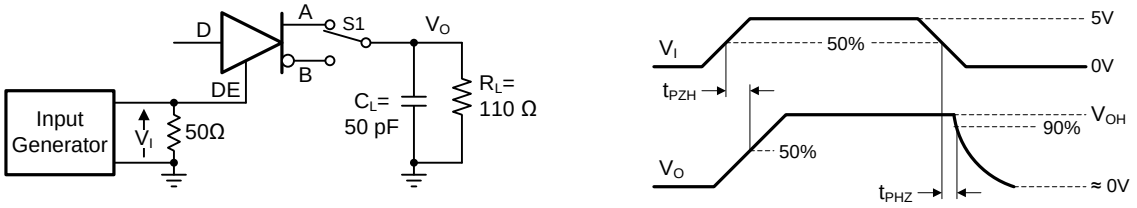


Figure 7. Measurement of Driver Enable and Disable Times With Active-High Output and Pull-Down Load

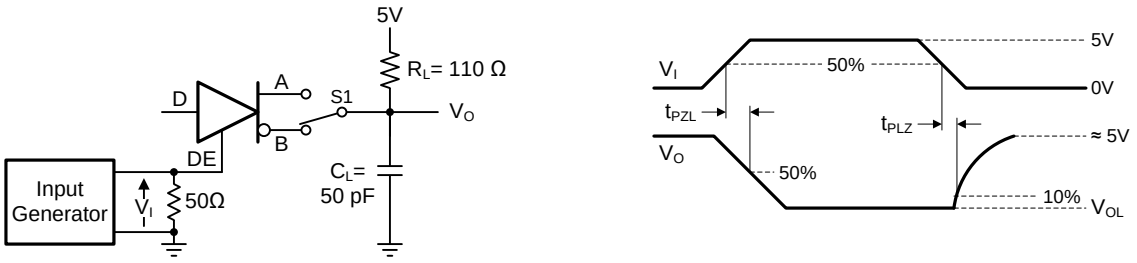


Figure 8. Measurement of Driver Enable and Disable Times With Active-Low Output and Pull-up Load

7.2 Receiver

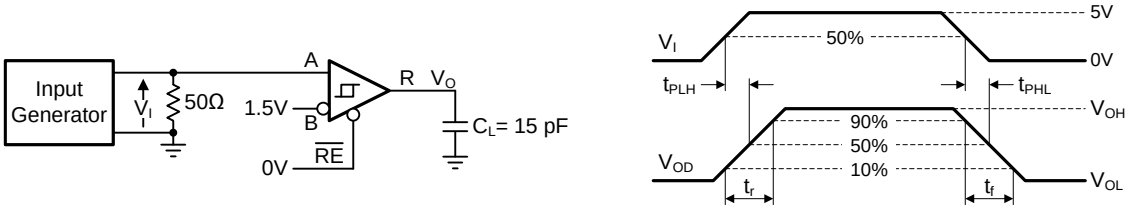


Figure 9. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

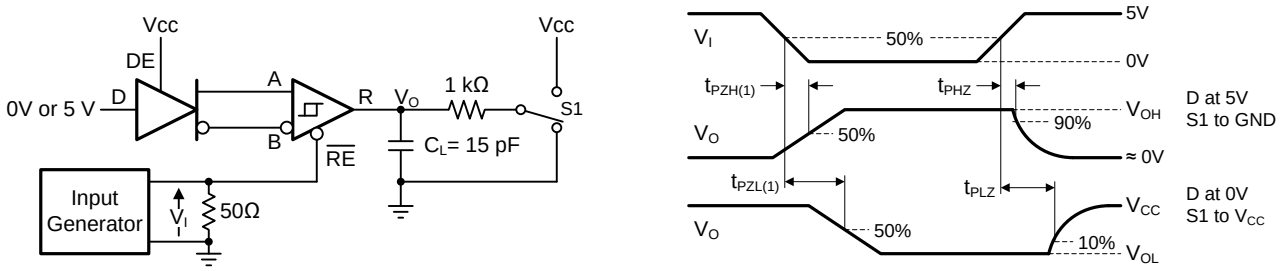


Figure 10. Measurement of Receiver Enable and Disable Times With Driver Enabled

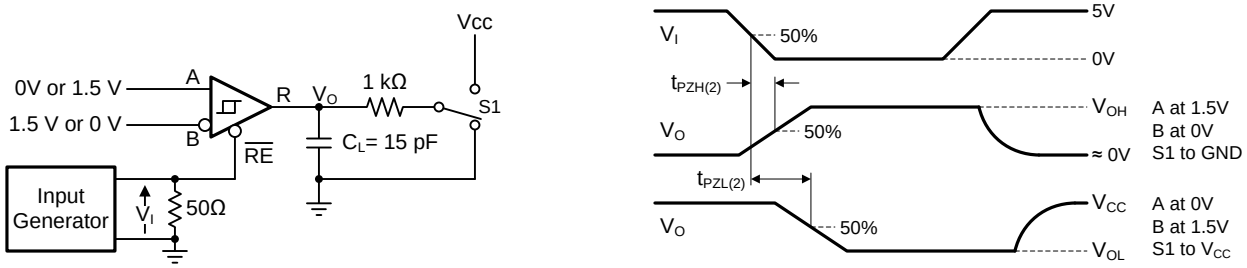


Figure 11. Measurement of Receiver Enable Times With Driver Disabled

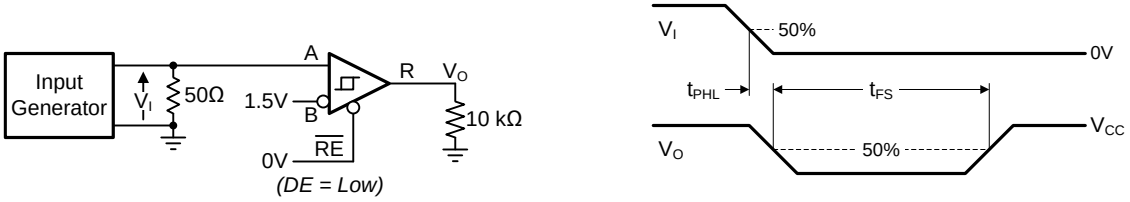


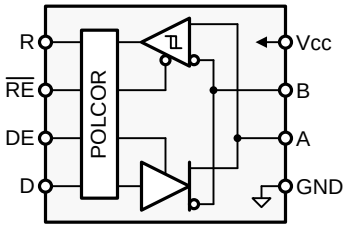
Figure 12. Measurement of Receiver Polarity-Correction Time With Driver Disabled

8 Detailed Description

8.1 Overview

The SN65HVD888 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 250 kbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand up ESD strikes up to 12 kV (per IEC 61000-4-2) and EFT transients up to 4 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of SN65HVD82 may share a common RS-485 bus due to the device's low bus input currents. The device features automatic polarity correction, which detects bus mis-wirings at start-up and then swaps the *A* and *B* halves of the bus if needed.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low-Power Standby Mode

When the driver and the receiver are both disabled (DE = Low and RE = High) the device enters standby mode. If the enable inputs are in the disabled state for only a brief time (for example: less than 100 ns), the device does not enter standby mode, preventing the SN65HVD888 from entering standby mode during driver or receiver enabling. Only when the enable inputs are held in the disabled state for a duration of 300 ns or more does the device enter low-power standby mode. In this mode most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active. During V_{CC} power-up, when the device is set for both driver and receiver disabled mode, the device may consume more than 5-µA of I_{CC} disabled current because of capacitance charging effects. This condition occurs only during V_{CC} power up.

8.3.2 Bus Polarity Correction

The SN65HVD888 automatically corrects a wrong bus-signal polarity caused by a cross-wire fault. In order to detect the bus polarity, all three of the following conditions must be met:

- A failsafe-biasing network (commonly at the master node) must define the signal polarity of the bus
- A slave node must enable the receiver and disable the driver ($\overline{RE}$ = DE = Low)
- The bus must idle for the failsafe time, $t_{FS\text{-}max}$

After the failsafe time has passed, the polarity correction is complete and is applied to both the receive and transmit channels. The status of the bus polarity is latched within the transceiver and is maintained for subsequent data transmissions.

NOTE

Data string durations of consecutive 0s or 1s exceeding $t_{FS\text{-}min}$ can accidently trigger a wrong polarity correction and must be avoided.

Figure 13 shows a simple point-to-point data link between a master node and a slave node. Because the master node with the failsafe biasing network determines the signal polarity on the bus, an RS-485 transceiver without polarity correction, such as SN65HVD82, suffices. All other bus nodes, typically performing as slaves, require the SN65HVD888 transceiver with polarity correction.

Feature Description (continued)

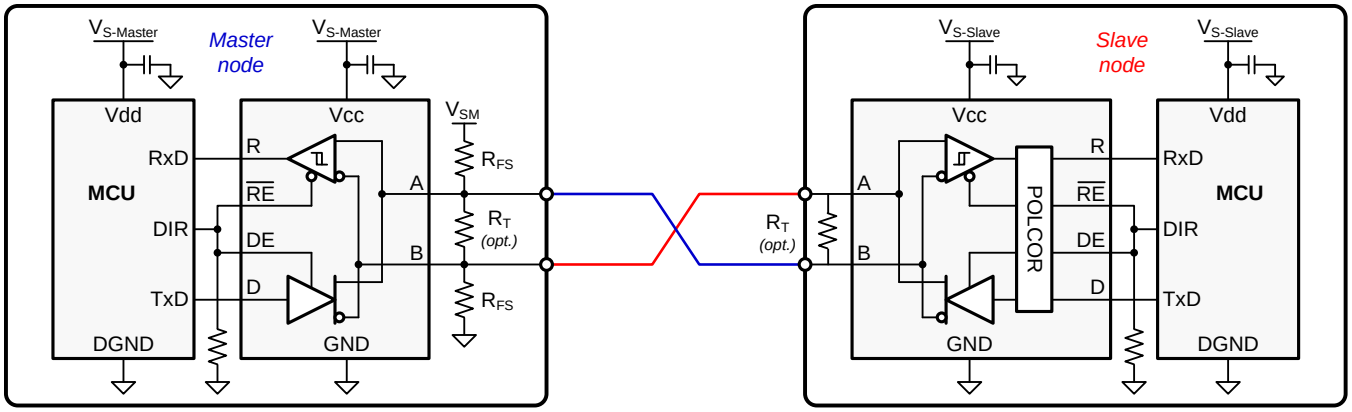


Figure 13. Point-To-Point Data Link With Cross-Wire Fault

Prior to initiating data transmission the master transceiver must idle for a time span that exceeds the maximum failsafe time, $t_{FS\text{-}max}$, of a slave transceiver. This idle time is accomplished by driving the direction control line, DIR, low. After a time, $t > t_{FS\text{-}max}$, the master begins transmitting data.

Because of the indicated cross-wire fault between master and slave, the slave node receives bus signals with reversed polarity. Assuming the slave node has just been connected to the bus, the direction-control pin is pulled-down during power-up and then is actively driven low by the slave MCU. The polarity correction begins as soon as the slave supply is established and ends after approximately 44 to 76 ms.

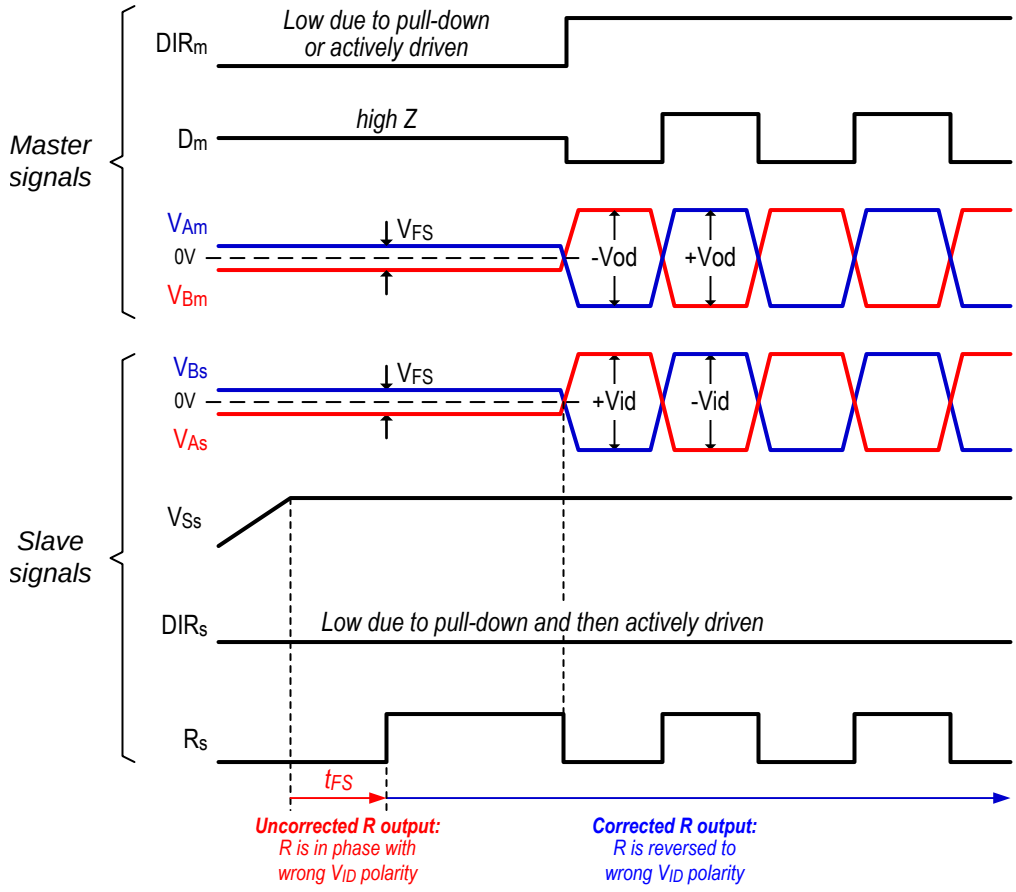


Figure 14. Polarity Correction Timing Prior to a Data Transmission

Feature Description (continued)

Initially the slave receiver assumes that the correct bus polarity is applied to the inputs and performs no polarity reversal. Because of the reversed polarity of the bus-failsafe voltage, the output of the slave receiver, R_S, turns low. After t_{FS} has passed and the receiver has detected the wrong bus polarity, the internal POLCOR logic reverses the input signal and R_S turns high.

At this point all incoming bus data with reversed polarity are polarity corrected within the transceiver. Because polarity correction is also applied to the transmit path, the data sent by the slave MCU are reversed by the POLCOR logic and then fed into the driver.

The reversed data from the slave MCU are reversed again by the cross-wire fault in the bus, and the correct bus polarity is reestablished at the master end.

This process repeats each time the device powers up and detects an incorrect bus polarity.

8.4 Device Functional Modes

Table 1. Driver Pin Functions

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus High
POLARITY-CORRECTING MODE (1)				
H	H	L	H	Actively drives bus Low
L	H	H	L	Actively drives bus High
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus Low

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when $\overline{RE}$ turns from Low to High.

Table 2. Receiver Pin Functions

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
NORMAL MODE			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state
POLARITY-CORRECTING MODE (1)			
$V_{IT+} < V_{ID}$	L	L	Receive valid bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	H	Receive polarity corrected bus High
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when $\overline{RE}$ turns from Low to High.

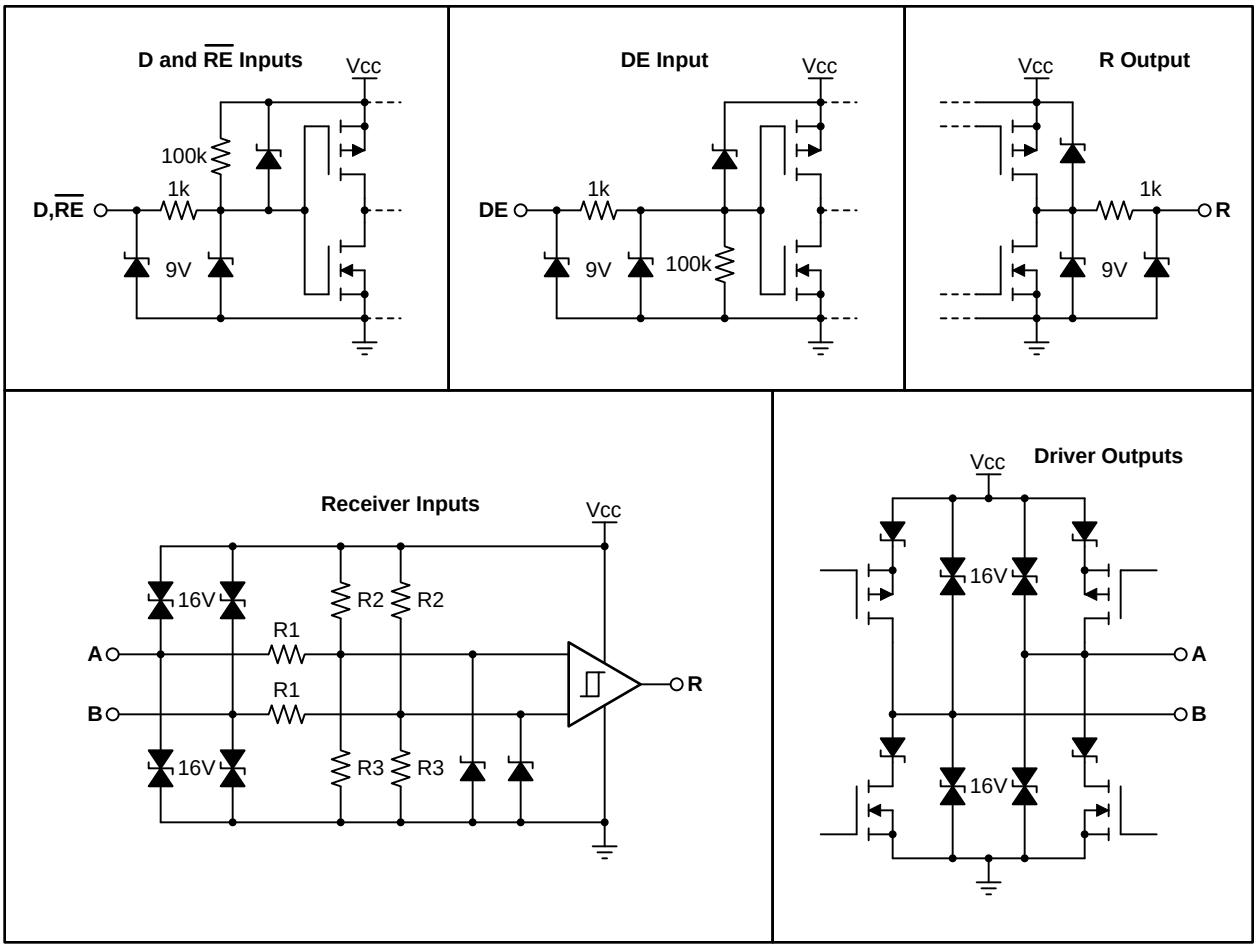


Figure 15. Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Device Configuration

The SN65HVD888 is a half-duplex RS-485 transceiver operating from a single 5-V ±10% supply. The driver and receiver enable pins allow for the configuration of different operating modes.

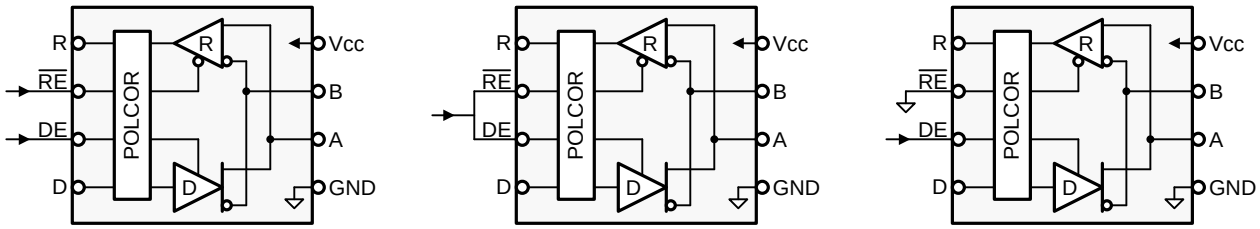


Figure 16. Transceiver Configurations

Using independent enable lines provides the most flexible control as the lines allow for the driver and the receiver to be turned on and turned off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not. Only this configuration allows the SN65HVD888 to enter low-power standby mode because it allows both the driver and receiver to be disabled simultaneously.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver enable to ground and controlling only the driver-enable input also uses only one control line. In this configuration a node not only receives the data on the bus sent by other nodes but also receives the data sent on the bus, enabling the node to verify the correct data has been transmitted.

9.1.2 Bus Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, RT, whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z0 = 100 Ω, and RS-485 cable with Z0 = 120 Ω. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

Application Information (continued)

Table 3. VID with a Failsafe Network and Bus Termination

V_{CC}	R_L DIFFERENTIAL TERMINATION	R_{FS} PULLUP	R_{FS} PULLDOWN	V_{ID}
5 V	54 Ω	560 Ω	560 Ω	230 mV
		1 KΩ	1 KΩ	131 mV
		4.7 KΩ	4.7 KΩ	29 mV
		10 KΩ	10 KΩ	13 mV

An external failsafe-resistor network must be used to ensure failsafe operation during an idle bus state. When the bus is not actively driven, the differential receiver inputs could float allowing the receiver output to assume a random output. A proper failsafe network forces the receiver inputs to exceed the V_{IT} threshold, thus forcing the SN65HVD888 receiver output into the failsafe (high) state. Table 3 shows the differential input voltage (V_{ID}) for various failsafe networks with a 54-Ω differential bus termination.

9.1.3 Cable Length Versus Data Rate

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

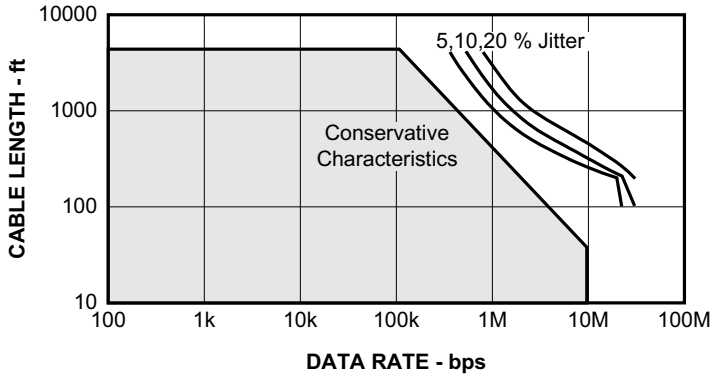


Figure 17. Cable Length vs Data Rate Characteristic

9.1.4 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for the short distance is because a stub presents a non-terminated piece of bus line which can introduce reflections if the distance is too long. As a general guideline, the electrical length or round-trip delay of a stub should be less than one-tenth of the rise time of the driver, thus leading to a maximum physical stub length of as shown in Equation 1.

$$L_{Stub} \leq 0.1 \times t_r \times v \times c$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s or 9.8×10^8 ft/s)
- v is the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of c (1)

Based on Equation 1, with a minimum rise time of 400 ns, Equation 2 shows the maximum cable-stub length of the SN65HVD888.

$$L_{Stub} \leq 0.1 \times 400 \times 10^{-9} \times 3\ 10^8 \times 0.78 = 9.4 \text{ m (or 30.6 ft)} \quad (2)$$

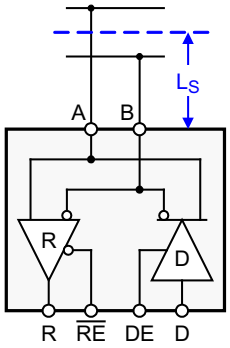


Figure 18. Stub Length

9.1.5 3- to 5-V Interface

Interfacing the SN65HVD888 to a 3-V controller is easy. Because the 5-V logic inputs of the transceiver accept 3-V input signals they can be directly connected to the controller I/O. The 5-V receiver output, R, however must be level-shifted by a Schottky diode and a 10-k resistor to connect to the controller input (see Figure 19). When R is high, the diode is reverse biased and the controller supply potential lies at the controller RxD input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2 V lies at the controller RxD input.

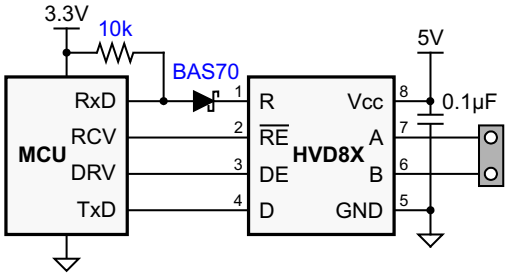


Figure 19. 3-V to 5-V Interface

9.1.6 Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ±200 mV. When the differential input voltage, V_{ID}, is greater than +200 mV, the receiver output turns high, for V_{ID} < –200 mV the receiver outputs low.

The SN65HVD888 transceiver implements high receiver noise-immunity by providing a typical positive-going input threshold of 35 mV and a minimum hysteresis of 40 mV. In the case of a noisy input condition therefore, a differential noise voltage of up to 40 mV_{PP} can be present without causing the receiver output to change states from high to low.

9.1.7 Transient Protection

The bus terminals of the SN65HVD888 transceiver family possess on-chip ESD protection against ±16 kV HBM and ±12 kV IEC61000-4-2 contact discharge. The International Electrotechnical Commision (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, C_S, and 78% lower discharge resistance, R_D of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

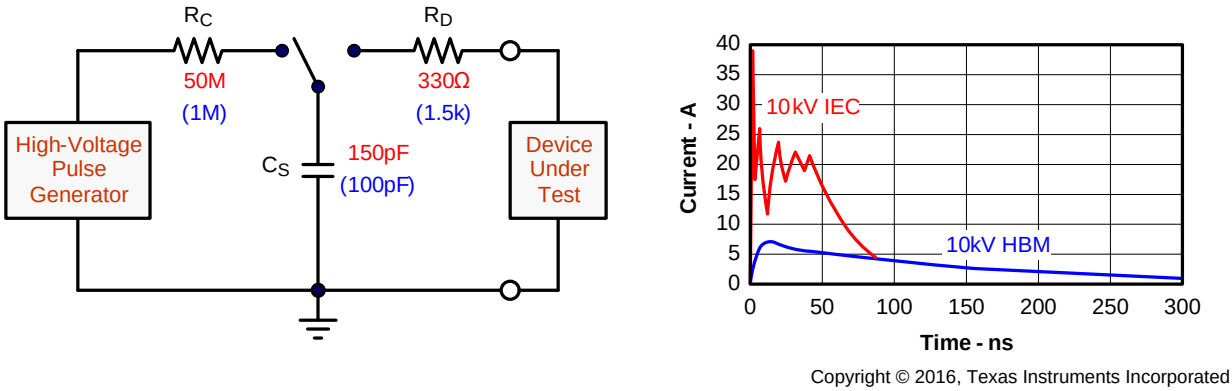


Figure 20. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients. Figure 12 suggests two circuit designs providing protection against short and long duration surge transients, in addition to ESD and Electrical Fast Transients (EFT) transients. Table 4 lists the bill of materials for the external protection devices.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 21 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. In the diagram on the left of Figure 21, the tiny blue blip in the bottom left corner represents the power of a 10-kV ESD transient, which already dwarfs against the significantly higher EFT power spike, and certainly dwarfs against the 500-V surge transient. This type of transient power is well representative of factory environments in industrial and process automation. The diagram on the fright of Figure 21 compares the enormous power of a 6-kV surge transient, most likely occurring in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient.

NOTE

The unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost dropping off the scale.

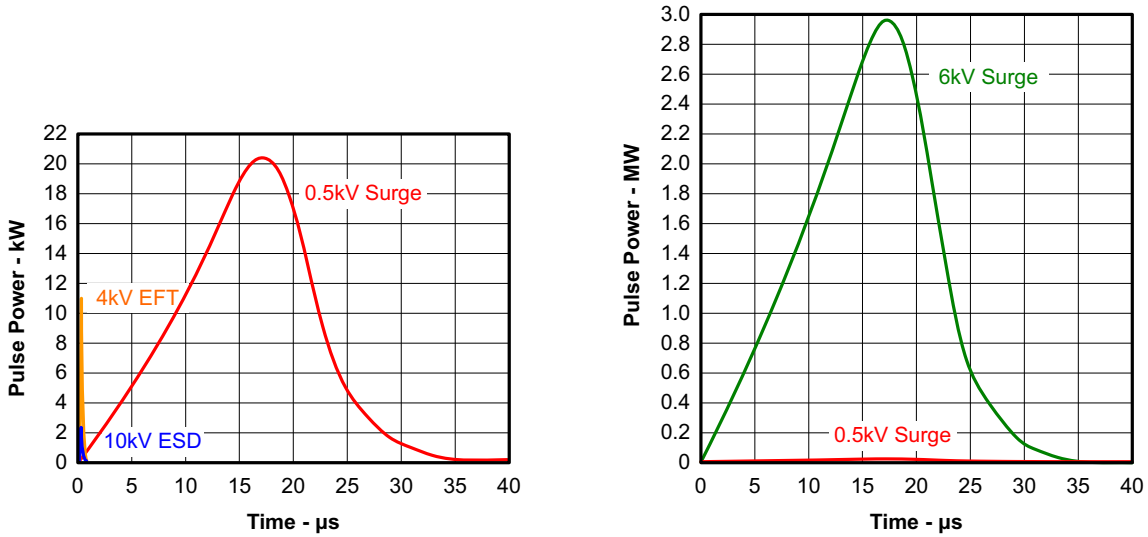


Figure 21. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, hgih-energy content is signified by long pulse duration and slow decaying pulse power

The electrical energy of a transient that is dumped into the internal protection cells of the transceiver is converted into thermal energy. This thermal energy heats the protection cells and literally destroys them, thus destroying the transceiver. Figure 22 shows the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

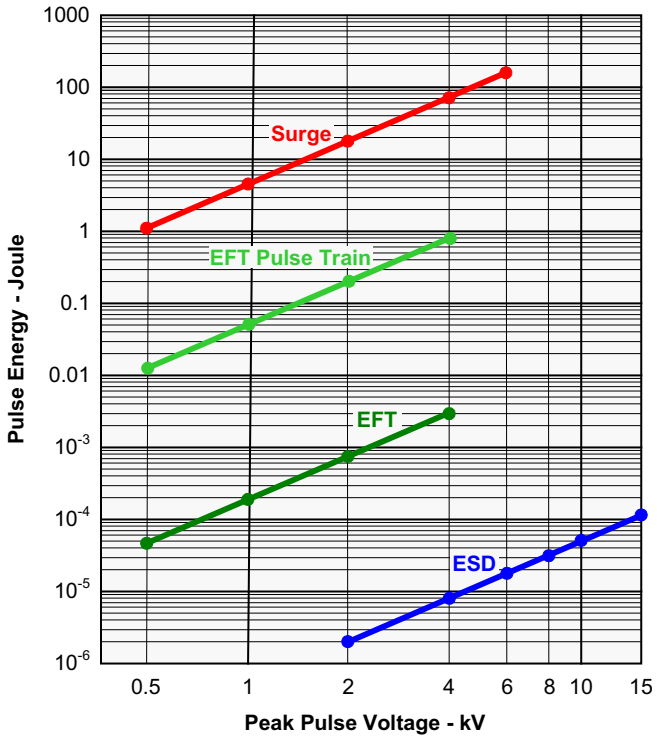


Figure 22. Comparison of Transient Energies

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, 250-kbps RS-485 Transceiver	SN65HVD888	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional.	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200mA Transient Blocking Unit 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns

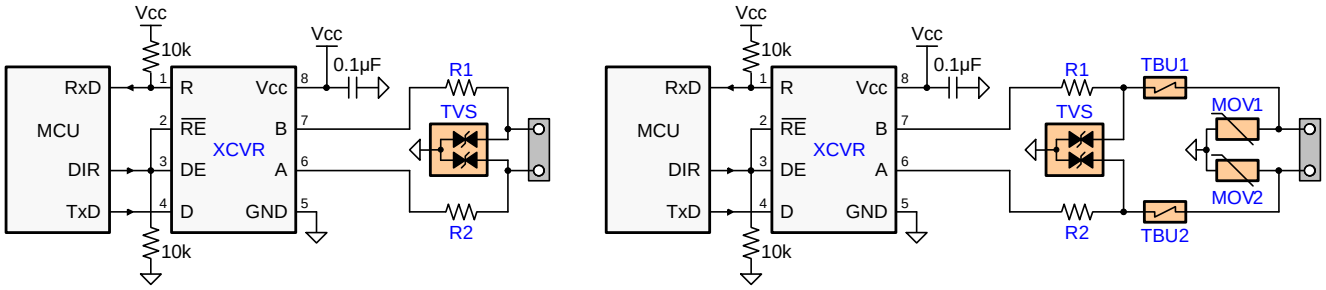
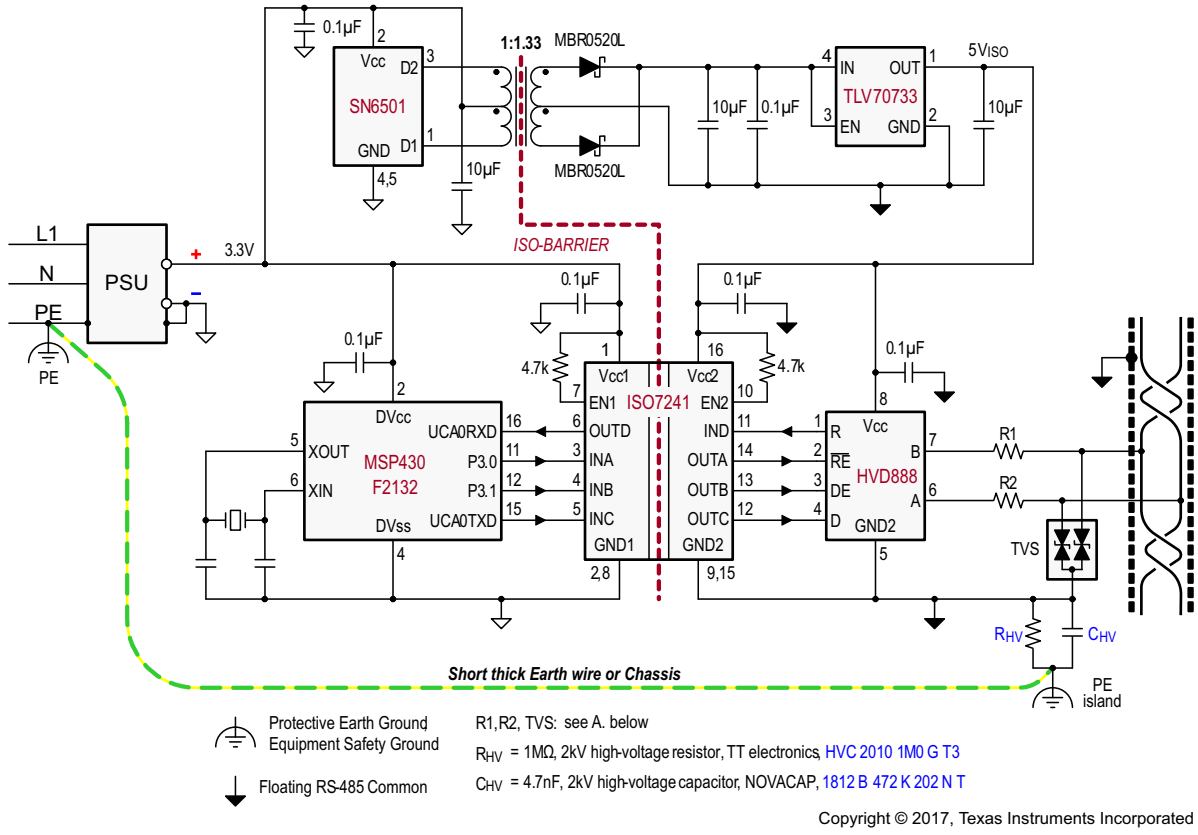


Figure 23. Transient Protections Against ESD, EFT, and Surge Transients

The left circuit shown in Figure 23 provides surge protection of ≥ 500-V transients, while the right protection circuits can withstand surge transients of 5 kV.

9.2 Typical Application

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver through a multi-channel, digital isolator (Figure 24).



A. See Table 4.

Figure 24. Isolated Bus Node With Transient Protection

9.2.1 Design Requirements

Example Application: Isolated Bus Node with Transient Protection

- RS-485-compliant bus interface (needs differential signal amplitude of at least 1.5 V under fully-loaded conditions – essentially, maximum number of nodes connected and with dual 120-Ω termination).
- Galvanic isolation of both signal and power supply lines.
- Able to withstand ESD transients up to 12 kV (per IEC 61000-4-2) and EFTs up to 4 kV (per IEC 61000-4-4).
- • Full control of data flow on bus in order to prevent contention (for half-duplex communication).

9.2.2 Detailed Design Procedure

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-kΩ resistors to limit input currents during transient events.

While the transient protection is similar to the one in Figure 23 (left circuit), an additional high-voltage capacitor diverts transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This diversion is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Typical Application (continued)

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

9.2.3 Application Curve

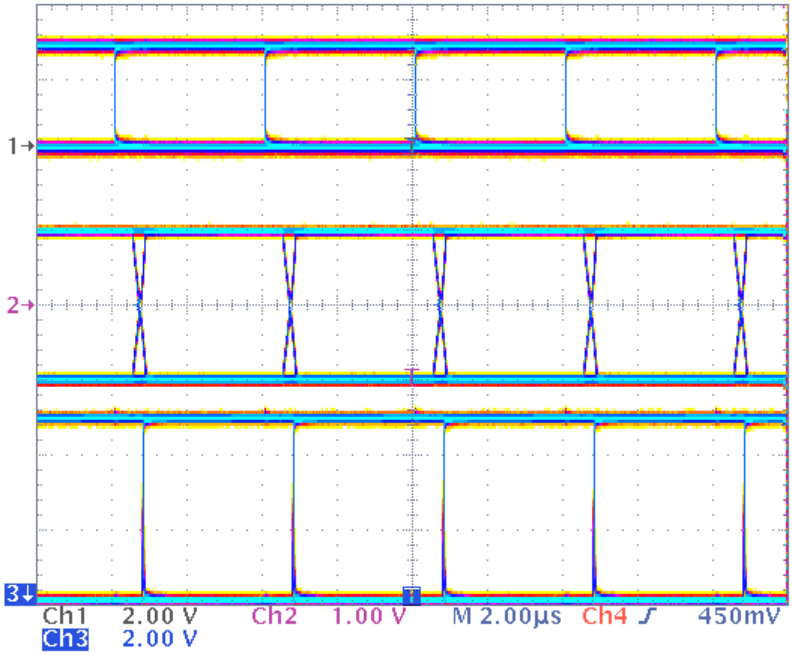


Figure 25. SN65HVD888 D Input (Top), Differential Output (Middle), and R Output (Bottom), 250 kbps Operation, PRBS Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Design and Layout Considerations For Transient Protection

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for PCB design to be successful, begin with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100- to 220-nF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1- to 10-k pullup or pulldown resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
   - While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few-hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

11.2 Layout Example

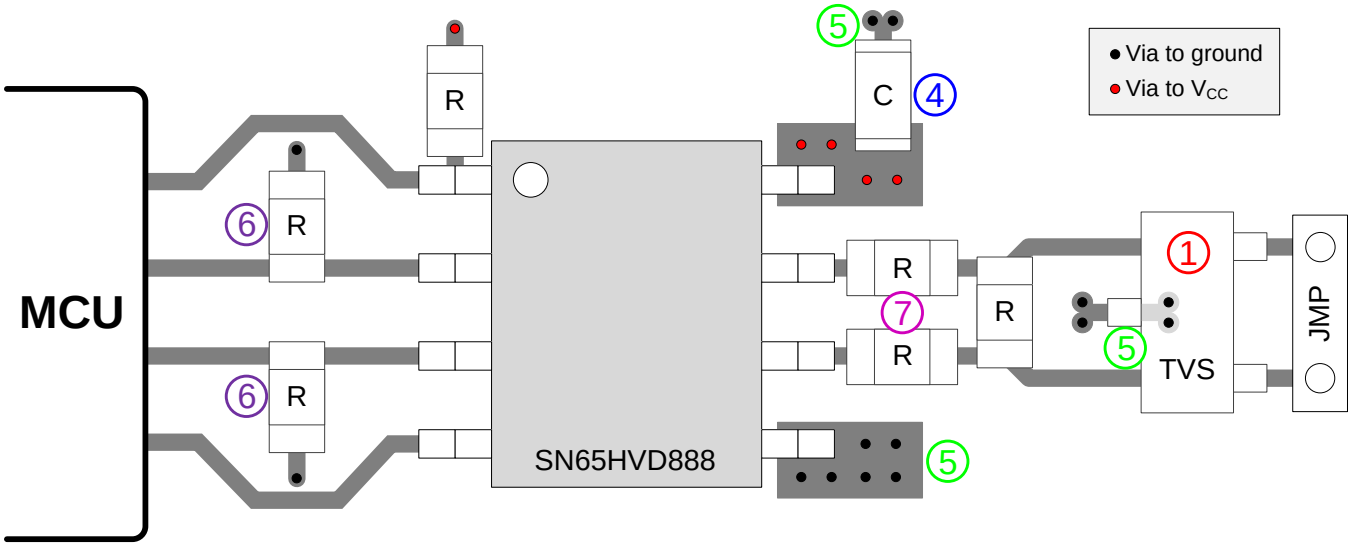


Figure 26. SN65HVD888 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD888D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888	Samples
SN65HVD888DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

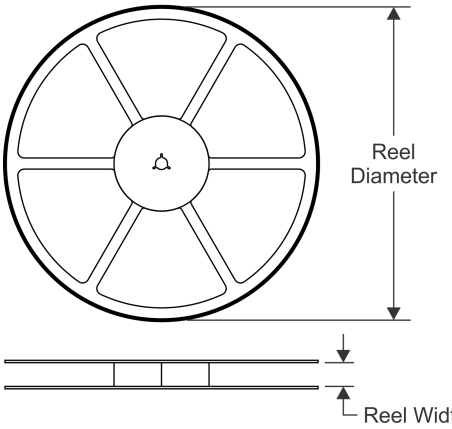
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

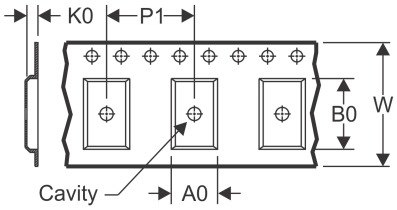
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

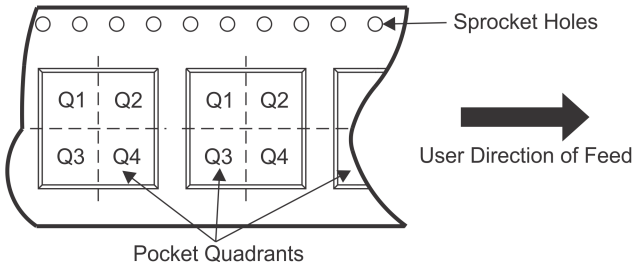


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

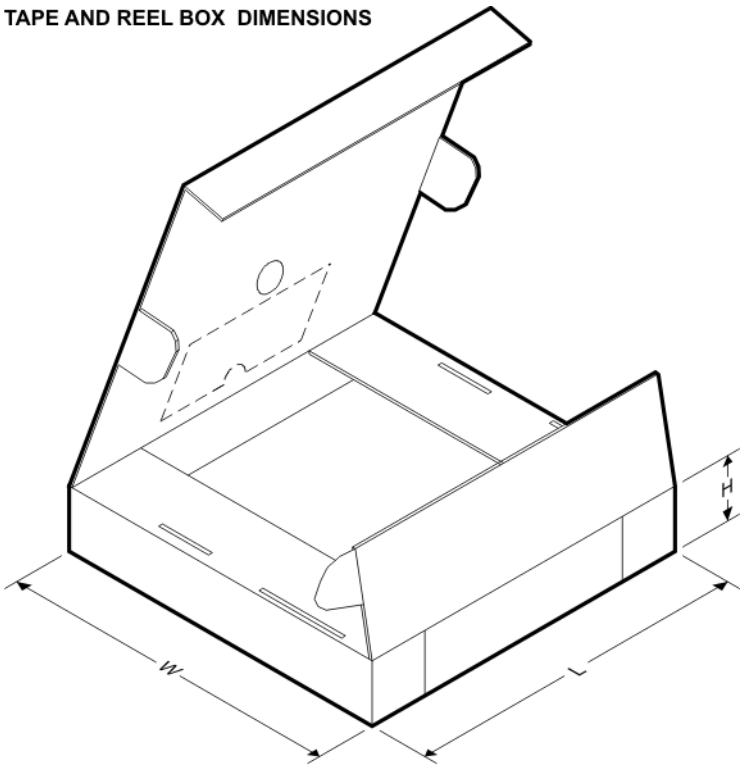
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD888DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

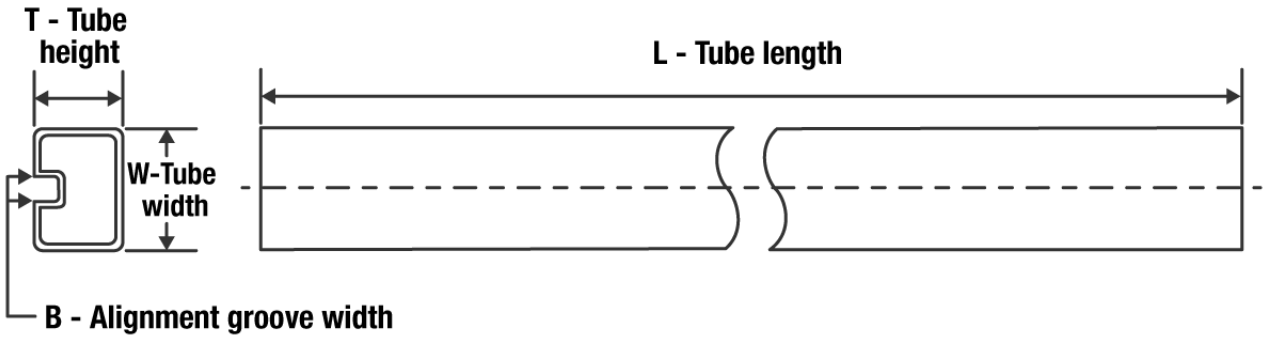
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

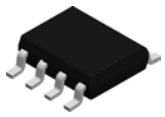
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD888DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD888D	D	SOIC	8	75	507	8	3940	4.32

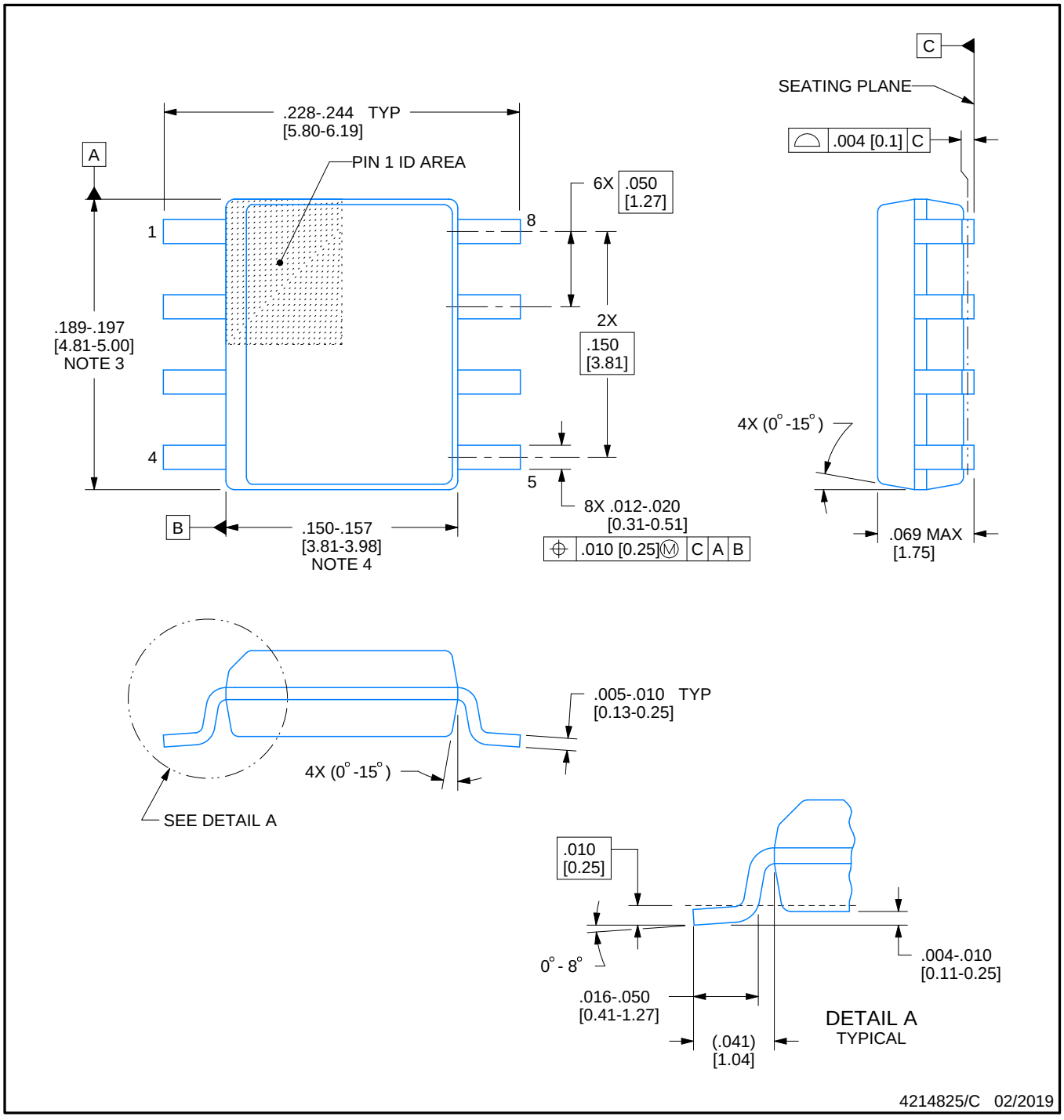


PACKAGE OUTLINE

D0008A

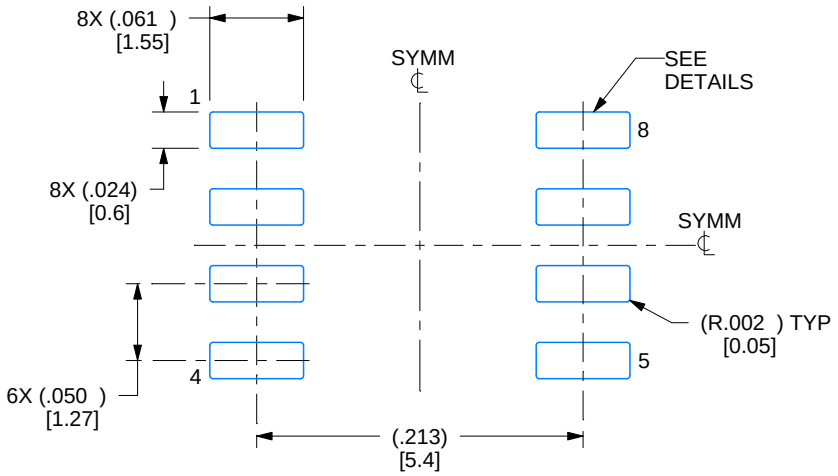
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

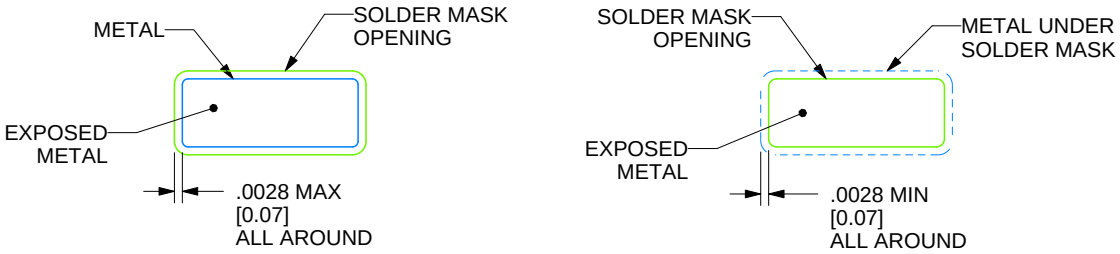


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

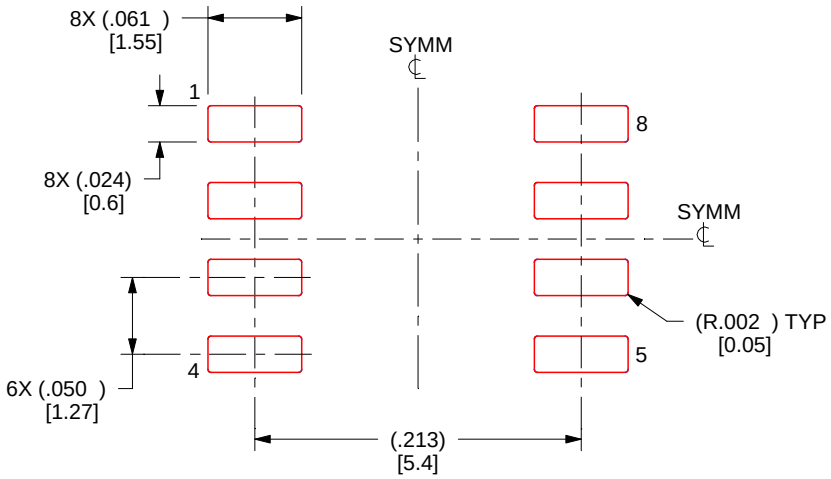
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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