M08886-13

High Performance RGB LED/Laser Driver for LCD/LCoS/DLP Projection Displays

Rev V1

Features

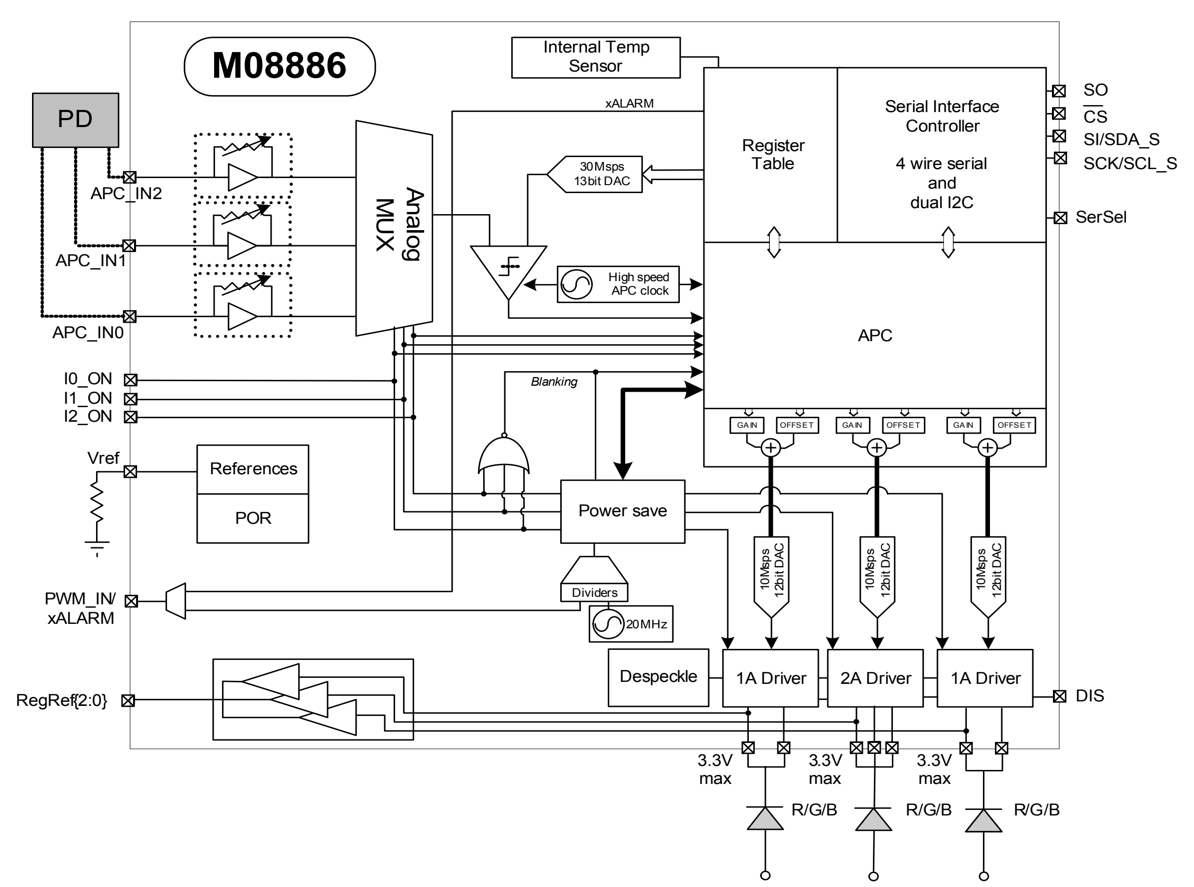
- One 2A common anode LED/Laser driver
- Two 1A common anode LED/Laser drivers
- Laser Despeckle
- Integrated 30Msps 12bit DACs
- Automatic real time power control (ColorMinder)
- DC-DC converter reference generators to optimize each laser bias voltage
- High speed 4 wire interface or slave I^{2}C for register settings download from µC

Applications

- LCD/LCoS/DLP Portable and Pico Projectors

The M08886 is a high efficiency integrated RGB LED/Laser driver with patent pending de-speckle and power save technologies for LCD/LCoS/DLP projection displays. It features ColorMinder - a multilevel automatic laser power control for consistent white balance across temperature variation and laser aging. The M08886 allows for the monitoring of the internal IC junction temperature and the control of external DC-DC converters to generate optimal laser supply.

Block Diagram



M08886
Internal Temp Sensor
xALARM
PD
APC_IN2
APC_IN1
APC_IN0
Analog MUX
30Msps 13bit DAC
Register Table
Serial Interface Controller
4 wire serial and dual I2C
SO
CS
SI/SDA_S
SCK/SCL_S
SerSel
High speed APC clock
APC
Blanking
I0_ON
I1_ON
I2_ON
Vref
References
POR
Power save
GAIN
OFFSET
10Msps 12bit DAC
Dividers
20MHz
PWM_IN/ xALARM
RegRef{2:0}
Despeckle
1A Driver
2A Driver
1A Driver
DIS
3.3V max
R/G/B

Ordering Information

Part Number	Package	Operating Temperature
M08886G-13*		-40 °C to 85 °C
* The letter “G” designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.		

Revision History

Revision	Level	Date	Description
V1	Release	May 2015	Update register references.
F (V3P)	Preliminary	September 2010	Update specifications to match characterization data. Edit Functional Description and Register sections.
D (V2P)	Preliminary	June 2010	Corrected pin 21 and 22 description in Table 1-11.
C (V1P)	Preliminary	May 2010	Remove support for external EEPROM and Analog APC. Power dissipation and APC specifications updated. Functional Description updated.
B (V2A)	Advance	June 2009	Changed Format, content unchanged
A (V1A)	Advance	March 2009	Initial release.

Datasheet Font Conventions

Font	Example	Explanation
Italics	*IOUT0*	Words in Italics designate M08886 pins. In this case pin IOUT0.
Bold letter “x”	*IOUT**X*** apc**x**_ctrl0[2:1]	A letter “x” or “X” in bold font is a placeholder for channel 0, 1 or 2. When an “x” is used the information applies to all 3 channels. *IOUT**X*** can mean *IOUT0*, *IOUT1* or *IOUT2* or it can mean *OUT0*, *IOUT1* and *IOUT2* depending on the context. apc**x**_ctrl0[2:1] can mean registers apc0_ctrl0[2:1], apc1_ctrl0[2:1] or apc2_ctrl0[2:1] or registers apc0_ctrl0[2:1], apc1_ctrl0[2:1] and apc2_ctrl0[2:1] depending on the context

Table of Contents

Ordering Information 2
Revision History 2
Datasheet Font Conventions 2
Table of Contents 3
List of Figures 5
List of Tables 6
1.0 Product Specification 7
  1.1 Absolute Maximums 7
  1.2 DC Characteristics 8
  1.3 Target DAC (RGB sensor target current) 9
  1.4 Laser Current DACs 10
  1.5 Laser Drivers 14
  1.6 DC-DC Converters Reference Generators 14
  1.7 APC Input Characteristics 16
  1.8 CMOS Pins Characteristics 16
  1.9 Slave I2C Timing Specifications1,2 17
  1.10 High Speed Serial Interface Timing Specifications 18
  1.11 M08886 Pinout 20
  1.12 Pin List and Descriptions 21
  1.13 Package Information 22
2.0 Functional Description 23
  2.1 Automatic Power Control (APC) 23
    2.1.1 Simple Implementation of APC Control 24
    2.1.2 Highly Featured Implementation of APC Control 25
    2.1.3 Compensating the TIA at the Photodetector Input 26
    2.1.4 Laser Offset (threshold) Tracking with APC 27
  2.2 LASER/LED Current DACs 27
    2.2.1 Increasing the Maximum LED/Drive Current by Combining Outputs 28
  2.3 Laser\LED Voltage Supply Control 28
  2.4 Pulse Width Modulation (PWM) 31
  2.5 Multi Pulse Generator (MPG) 31

2.6 Power Save Features 33
2.7 Safety 33
2.8 Programmable Serial Interface 34
2.9 Driving a String of LEDs from a High Voltage Supply 34
2.10 Power Sequencing. 36
2.11 Layout Considerations. 36
3.0 Registers 37

List of Figures

Figure 1-1. Typical IOUT0 Current vs Headroom. 11
Figure 1-2. Typical IOUT1 Current vs Headroom. 12
Figure 1-3. Typical IOUT2 Current vs Headroom. 13
Figure 1-4. Typical IOUT0 Current with DC-DC Converter Controlled by REGREF0 15
Figure 1-5. Slave I2C Timing 17
Figure 1-6. Serial Interface Sequential Write 18
Figure 1-7. Serial Interface Random Write. 18
Figure 1-8. Serial Interface Sequential Read 19
Figure 1-9. Serial Interface Random Read. 19
Figure 1-10. M08886 Pinout. 20
Figure 1-11. Sawn QFN32 Package Information 22
Figure 2-1. laser/led Supply Control Block Diagram. 29
Figure 2-2. Controlling Laser/LED Supply with Three DC-DC Converters. 29
Figure 2-3. Controlling Laser/LED Supply with Single DC-DC Converter 30
Figure 2-4. Multi Pulse Generator Timing. 32
Figure 2-5. Driving a String of LEDs from a High Voltage Supply 35
Figure 2-6. Power-Up 36
Figure 2-7. Power-Down. 36

List of Tables

Table 1-1. Absolute Maximum Ratings 7
Table 1-2. DC Characteristics 8
Table 1-3. Register Settings used for Measurements in Various Operating Modes 9
Table 1-4. Target DAC 9
Table 1-5. Laser Current DACs 10
Table 1-6. Laser Drivers 14
Table 1-7. DC-DC Converters Reference Generators 14
Table 1-8. APC Input Characteristics 16
Table 1-9. CMOS Pins Characteristics 16
Table 1-10. Slave I2C Timing Specifications 17
Table 1-11. High Speed Serial Interface Timing Specifications 18
Table 1-12. Pin List and Descriptions 21
Table 2-1. Basic Register Configuration for APC Control 24
Table 2-2. Highly Featured Register Configuration for APC Control 25
Table 2-3. Clock Selection for PWM and MPG 31
Table 3-1. M08886 Registers 37

1.0 Product Specification

1.1 Absolute Maximums

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
DV_{DD}, ALV_{DD}	1.8 V Digital and Analog Supplies	1.98	V
DHV_{DD}, AHV_{DD}	3.3 V Digital and Analog Supplies	3.63	V
IOUT0, IOUT1, IOUT2	Output pins for driving LED/Laser - maximum voltage	3.3	V
T_{JCTN}	Junction Temperature	-40 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
$I^2C/\overline{SPI}$	Serial data format select input	-0.4 to 3	V
APC_IN0, APC_IN1, APC_IN2	RGB Photodiode Feedback Input Voltage	-0.4 to ALV_{DD} + 0.4	V
I_{APC_IN0}, I_{APC_IN1}, I_{APC_IN2}	RGB Photodiode Feedback Input Current	-0.5 to 4	mA
I_VREF	Current into Reference Voltage Pin	-0.12 to +0.12	mA
DIS	Disable all LED/Laser outputs	-0.4 to 3	V
I0_ON, I1_ON, I2_ON	Enable LED/Laser output	-0.4 to 3	V
CLK_IN, $\overline{CS}$, SI, SCLK, SO	SPI inputs and output	-0.4 to 3	V
SCLK_S, SDA_S	I^2C interface	-0.4 to 3	V
REGREF_0, REGREF_1, REGREF_2	External DC-DC converter control signal	-0.4 to DV_{DD} +0.4	V
I_REGREF_0, I_REGREF_1, I_REGREF_2	Current into or out of REGREFX pins	-0.12 to +0.12	mA

1.2 DC Characteristics

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted.

Typical values: Tc=25 °C, DV_{DD}=1.8 V, ALV_{DD}=1.8 V, DHV_{DD} =3.3 V, AHV_{DD} =3.3 V unless otherwise noted.

Table 1-2. DC Characteristics

Symbol	PARAMETER	CONDITIONS	Min	Typ	Max	Units
DV_{DD}	1.8 V supply for digital circuitry		1.71	1.8	1.89	V
ALV_{DD}	1.8 V supply for analog circuitry		1.71	1.8	1.89	V
DHV_{DD}	3.3 V supply for digital circuitry		3.13	3.3	3.47	V
AHV_{DD}	3.3 V supply for analog circuitry		3.13	3.3	3.47	V
I_{LVDD}	LED Mode Supply Current - 1.8 V (DV_{DD} and ALV_{DD})[1]	Open Loop LED Mode		17	27	mA
		Closed Loop LED Mode		31.5	45	
	Laser Mode Supply Current - 1.8 V (DV_{DD} and ALV_{DD})[1] (Despeckle enabled on IOUT0)	Open Loop Laser Mode		42	55	
		Closed Loop Laser Mode		53	87	
	Standby Current - 1.8 V	Standby Mode		5		
I_{HVDD}	LED Mode Supply Current - 3.3 V (DHV_{DD} and AHV_{DD})[1]	Open Loop LED Mode		7	11.1	mA
		Closed Loop LED Mode		7	12.1	
	Laser Mode Supply Current - 3.3 V (DHV_{DD} and AHV_{DD})[1] (Despeckle enabled on IOUT0)	Closed Loop Laser Mode		21.5	36	
		Closed Loop Laser Mode		20	35	
	Standby Current - 3.3 V			0.05		
Tc	Case Temp.	Measured on top of M08886 case	-40		85	°C

NOTES:

[1] Excludes serial interface (SPI/I^2C) current and LED/Laser current

Table 1-3. Register Settings used for Measurements in Various Operating Modes

Operating Mode	Register Settings
Open Loop LED Mode	0x00h=40h, 0x02h=08h, 0x08h=0Fh, 0x09h=0Eh, 0x0Fh=0Ah, 0x0Ah=0Eh, 0x0Bh=0Eh, 0x0Eh=01h, 0x1Ah=00h, 0x1Dh=00h, 0x26h=FFh, 0x28h=03h, 0x40h= 06h
Open Loop Laser Mode	0x00h=40h, 0x02h=00h, 0x08h=0Fh, 0x09h=0Eh, 0x0Ah=0Eh, 0x0Bh=0Eh, 0x0Eh=01h, 0x0Fh=0Ah, 0x17h=40h, 0x18h=00h, 0x1Ah=54h, 0x1Dh=11h, 0x26h=FFh, 0x28h=00h, 0x40h= 06h
Standby Mode	0x00h=40h, 0x02h=08h, 0x04h=00h, 0x05h=00h, 0x06h=00h, 0x07h=00h, 0x08h=01h, 0x09h=01h, 0x0Ah=01h, 0x0Bh=01h, 0x0Ch=40h, 0x0Eh=01h, 0x0Fh=0Ah, 0x26h=FFh, 0x40h= 06h,0x90h=10h
Closed Loop LED Mode	0x00h=00h, 0x02h=08h, 0x04h=00h, 0x05h=00h, 0x06h=00h, 0x07h=00h, 0x08h=0Fh, 0x09h=0Eh, 0x0Ah=0Eh, 0x0Bh=0Eh 0x0Eh=00h, 0x0Fh=0Ah, 0x1Ah=00h, 0x1Dh=00h, 0x28h=03h, 0x38h=F4h, 0x3Ch=F2h, 0x40h=F0h, 0x41h=3Ch, 0x90h=00h
Closed Loop Laser Mode	0x00h=00h, 0x02h=00h, 0x04h=00h, 0x05h=00h, 0x06h=00h, 0x07h=00h, 0x08h=0Fh, 0x09h=0Eh, 0x0Ah=0Eh, 0x0Bh=0Eh 0x0Eh=00h, 0x0Fh=0Ah, 0x1Ah=54h, 0x1Dh=11h, 0x28h=00h, 0x32h=0Eh, 0x33h=00h, 0x38h=F4h, 0x3Ch=F2h, 0x40h=F0h, 0x41h=3Ch, 0x90h=00h

1.3 Target DAC (RGB sensor target current)

Typical values: Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-4. Target DAC

PARAMETER	CONDITIONS	Min	Typ	Max	Units
Resolution			13		bits
Conversion rate			30		Msps
Full scale monitor photodetector current			3.4		mA
Step size			412		nA

1.4 Laser Current DACs

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted.

Typical values: Tc=25 °C, DV_{DD}=1.8 V, ALV_{DD}=1.8 V, DHV_{DD} =3.3 V, AHV_{DD} =3.3 V unless otherwise noted.

Table 1-5. Laser Current DACs

PARAMETER	CONDITIONS	Min	Typ	Max	Units
Resolution			12		bits
Conversion rate			30		Msps
Full scale IOUT0	Current sunk at pin IOUT0 with bench power supply sourcing current and voltage adjusted so output headroom is 500 mV	1.85	2	2.25	A
Full scale IOUT1	Current sunk at pin IOUT1 with bench power supply sourcing current and voltage adjusted so output headroom is 500 mV	0.9	1.02	1.15	A
Full scale IOUT2	Current sunk at pin IOUT2 with bench power supply sourcing current and voltage adjusted so output headroom is 500 mV	0.85	0.98	1.15	A
IOUT0 step size	Average step size between 0.5A and 1.5A setting. Current is sourced from a bench power supply with the voltage adjusted for 500 mV headroom.	—	493	—	µA
IOUT1 step size	Average step size between 0.25A and 0.75A setting. Current is sourced from a bench power supply with the voltage adjusted for 500 mV headroom.	—	249	—	µA
IOUT2 step size	Average step size between 0.25A and 0.75A setting. Current is sourced from a bench power supply with the voltage adjusted for 500 mV headroom.	—	241	—	µA

Figure 1-1. Typical IOUT0 Current vs Headroom

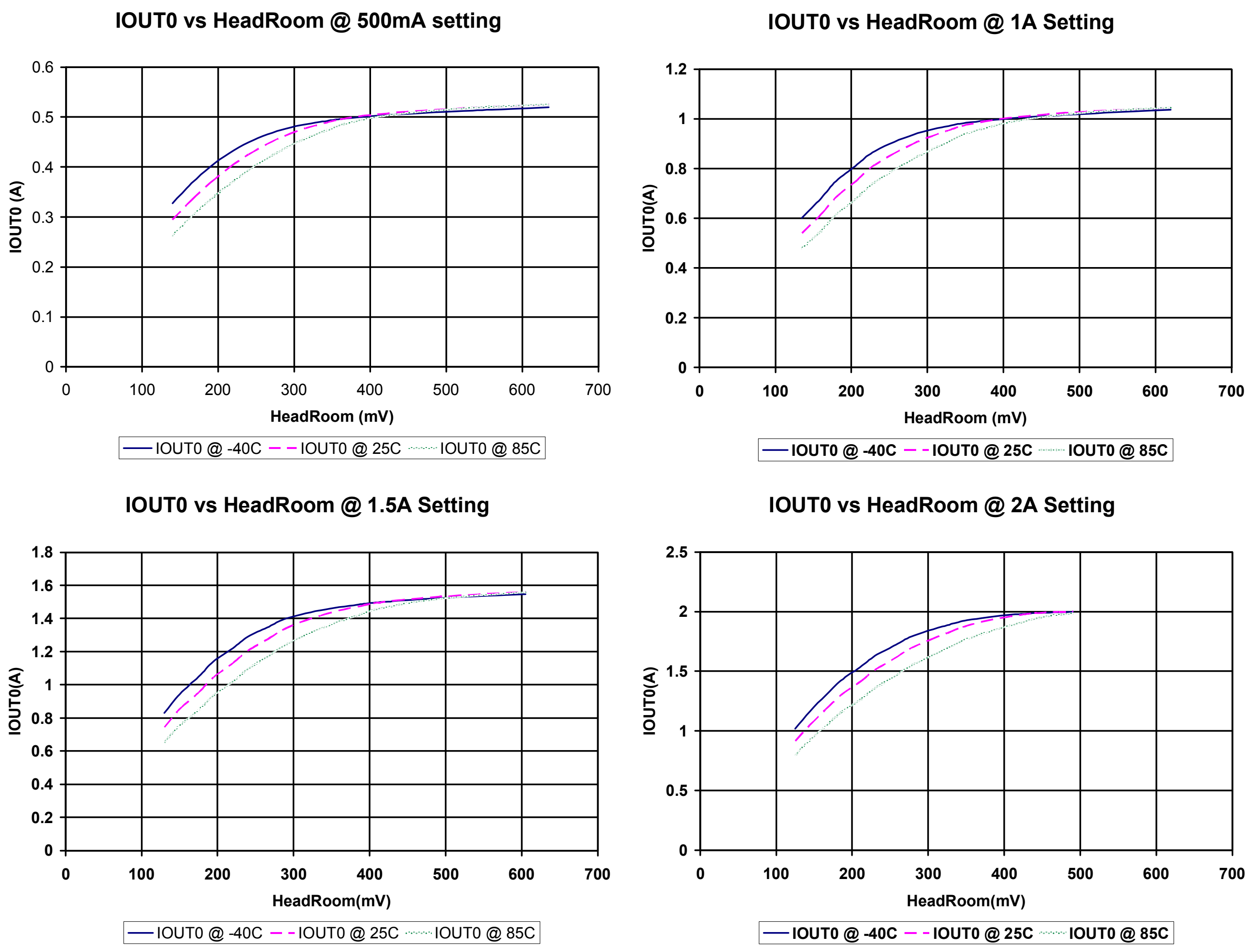


Figure 1-2. Typical IOUT1 Current vs Headroom

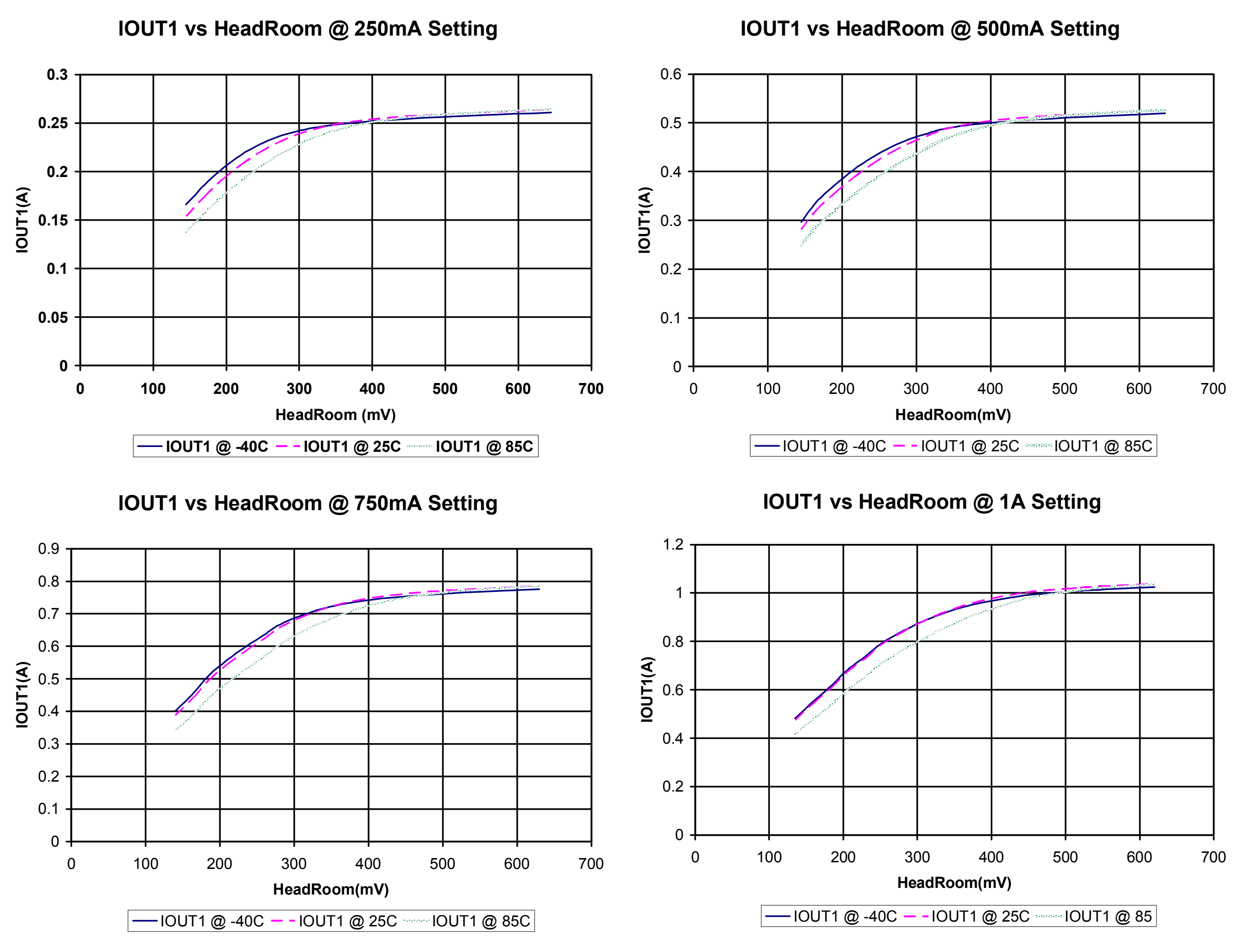
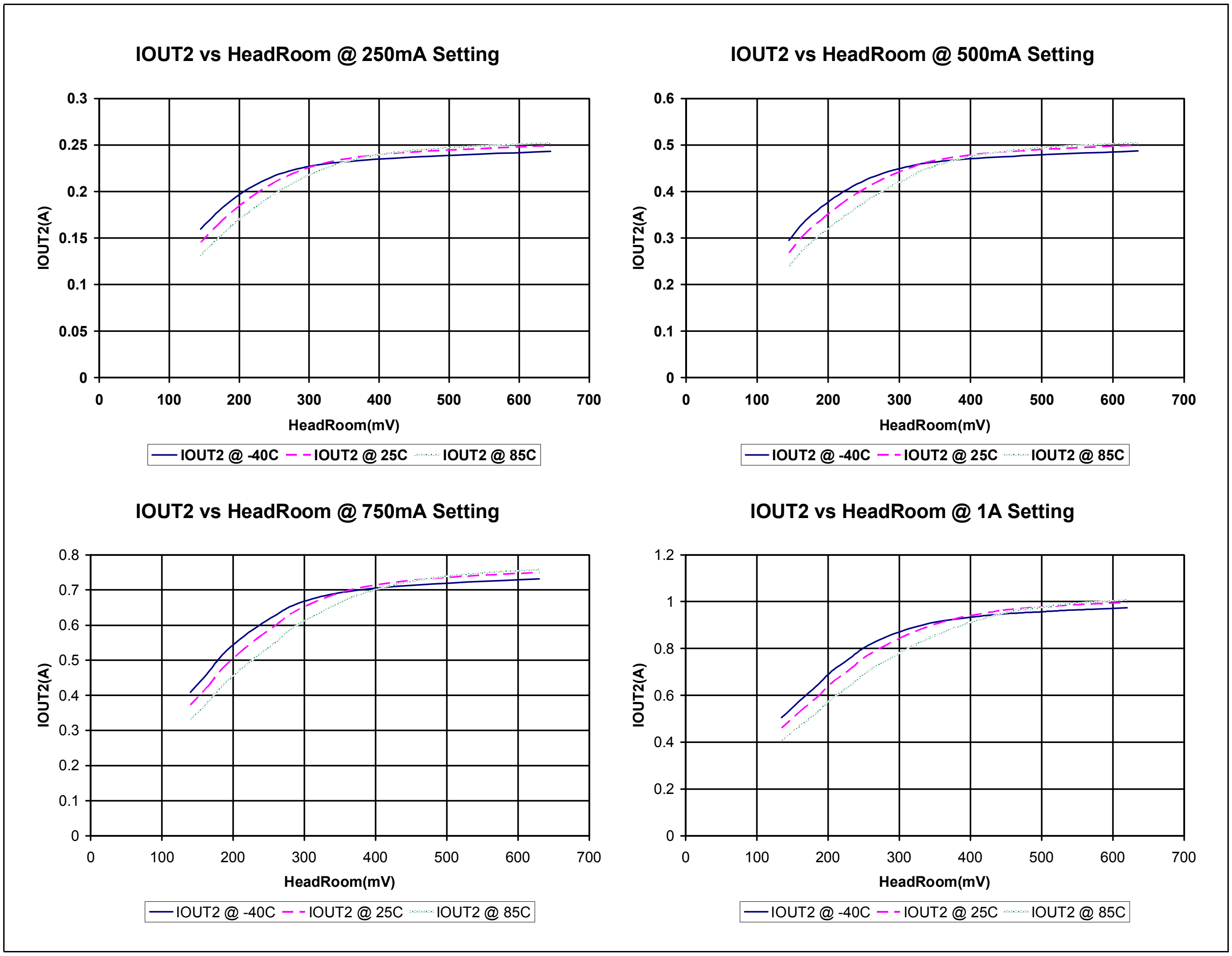


Figure 1-3. Typical IOUT2 Current vs Headroom



1.5 Laser Drivers

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted.

Typical values: Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-6. Laser Drivers

PARAMETER	CONDITIONS	Min	Typ	Max	Units
Maximum allowable voltage headroom[1]				3.3	V
Rise/fall time	20-80% Into 1 Ω electrical output			5	ns

NOTES:

[1] To prevent damage to the output devices the voltage drop across it cannot exceed 3.3 V. Please refer also to power sequencing paragraph and laser driver paragraph.

1.6 DC-DC Converters Reference Generators

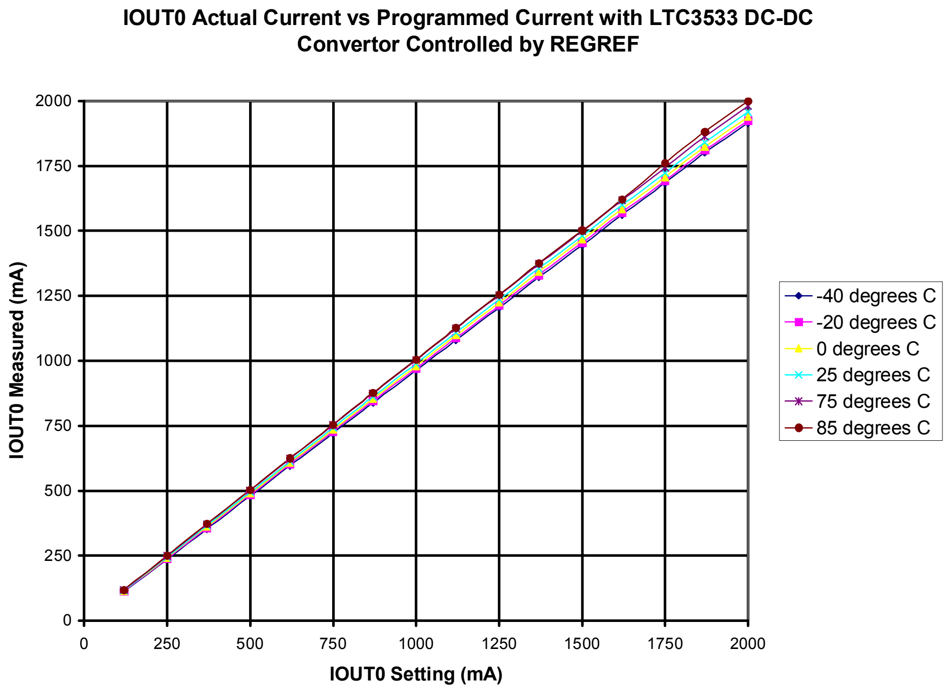
Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted.

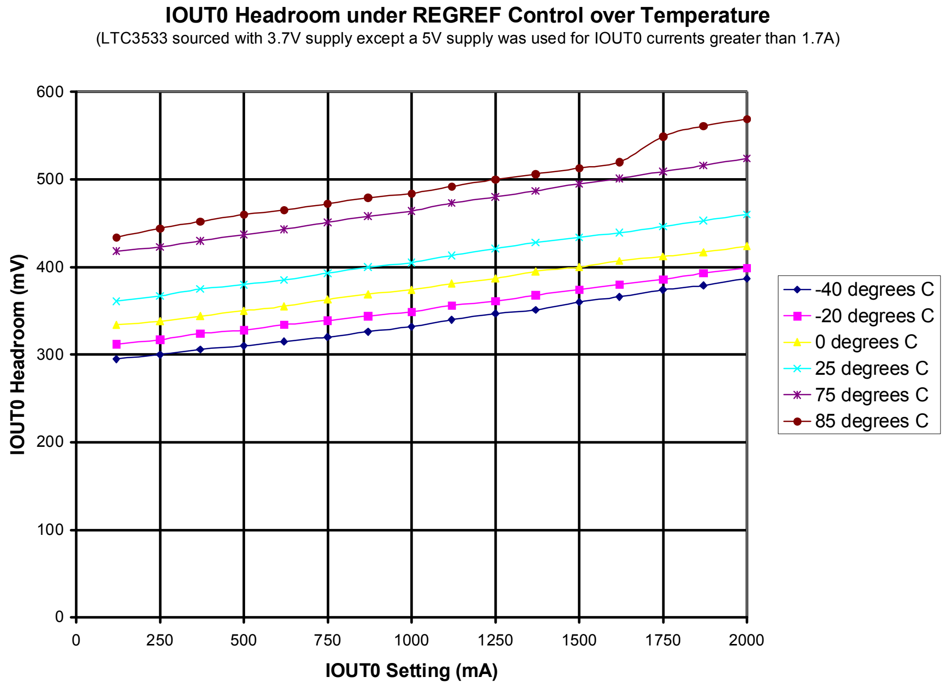
Typical values: Tc=25 °C, DV_{DD}=1.8 V, ALV_{DD}=1.8 V, DHV_{DD} =3.3 V, AHV_{DD} =3.3 V unless otherwise noted.

Table 1-7. DC-DC Converters Reference Generators

PARAMETER	CONDITIONS	Min	Typ	Max	Units
Voltage compliance	REGREF0,1,2	0.3	1.2	2.9	V
Maximum load capacitance	REGREF0,1,2			5	pF
Minimum resistive load	REGREF0,1,2	2.5			kΩ

Figure 1-4. Typical IOUT0 Current with DC-DC Converter Controlled by REGREF0





1.7 APC Input Characteristics

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted.

Typical values: Tc=25 °C, DV_{DD}=1.8 V, ALV_{DD}=1.8 V, DHV_{DD} =3.3 V, AHV_{DD} =3.3 V unless otherwise noted.

Table 1-8. APC Input Characteristics

PARAMETER	CONDITIONS	Min	Typ	Max	Units
Full scale input	APC_IN0,1,2		3.4		mA
PD capacitance[1]	APC_IN0,1,2			80	pF
Input bias	APC_IN0,1,2		$ALV_{DD}/2$		V
Maximum Voltage, APC_INX				1.98	V

NOTES:

[1] Care should be taken in routing of each PD input so that total capacitance on the pin including routing does not exceed 80 pF

1.8 CMOS Pins Characteristics

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted.

Typical values: Tc=25 °C, DV_{DD}=1.8 V, ALV_{DD}=1.8 V, DHV_{DD} =3.3 V, AHV_{DD} =3.3 V unless otherwise noted.

Table 1-9. CMOS Pins Characteristics

PARAMETER	CONDITIONS	Min	Typ	Max	Units
V_{IH}[1]		0.65 DV_{DD}		2.75	V
V_{IL}		0		0.35 DV_{DD}	V
V_{OH}		DV_{DD}-0.4		DV_{DD}	V
V_{0L}		0		0.4	V
Rise/fall time[2]	Maximum load of 5 pF. SPI mode		3		ns

NOTES:

[1] Digital pins are (1.8 V devices) 2.5 V (+/-10%) tolerant

[2] In I^2C mode rise time depends on load and pull up resistor.

1.9 Slave I^{2}C Timing Specifications[1,2]

Typical values: Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-10. Slave I^{2}C Timing Specifications

Parameter	Symbol (refer to figure below)	Min	Typ	Max	Units
Clock Frequency, SCL_S	f_{SCL_SLAVE}	–	–	3.4	MHz
Clock Pulse Width Low	t_{LOW}	160	–	–	ns
Clock Pulse Width High	t_{HIGH}	60	–	–	ns
Clock Low to Data Out Valid	t_{AA}	0	–	70	ns
Start Hold Time	t_{HDSTA}	160	–	–	ns
Start Set-up Time	t_{SUSTA}	160	–	–	ns
Data In Hold Time	t_{HDDAT}	0	–	–	ns
Data In Set-up Time	t_{SUDAT}	10	–	–	ns
Outputs (SDA_M, SCL_M, SDA_S and SCL_S) internal pull-up resistor value[3]	$R_{PULL-UP}$	–	250	–	kΩ
Stop Set-up Time	t_{SUSTO}	160	–	–	ns
Data Out Hold Time	t_{DH}	5	–	–	ns

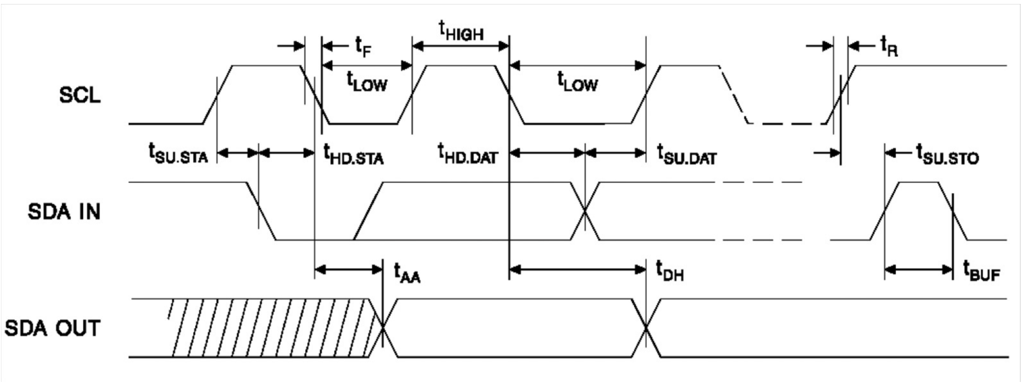
NOTES:

[1] Guaranteed by design and characterization.

[2] Specified at recommended operating conditions

[3] 4.7 kΩ should be added externally.

Figure 1-5. Slave I^{2}C Timing



1.10 High Speed Serial Interface Timing Specifications

Typical values: Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-11. High Speed Serial Interface Timing Specifications

Parameter	Symbol (refer to figure below)	Min	Typ	Max	Units
Clock Frequency	fclk=1/Tclk			40	MHz
Data in to clk hold time	Tdh	5			ns
Data in to clk set-up time	Tds	5			ns
Enable to clk set up time	Tcs	5			ns
Enable to clk hold time	Tch	5			ns
Read data output valid following rising edge of SCLK	Tdd	2		9	ns
SCLK duty cycle		45		55	%
NOTES: [1] Maximum output capacitance of 5 pF.					

Figure 1-6. Serial Interface Sequential Write

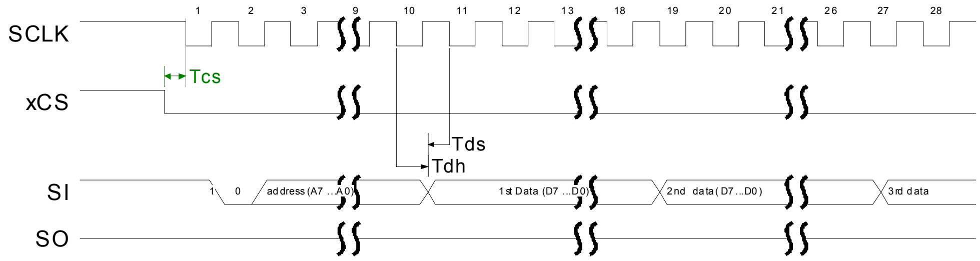

SCLK
1
2
3
9
10
11
12
13
18
19
20
21
26
27
28
Tcs
xCS
Tds
Tdh
SI
1
0
address (A7 ...A0)
1st Data (D7 ...D0)
2nd data (D7...D0)
3rd data
SO

Figure 1-7. Serial Interface Random Write

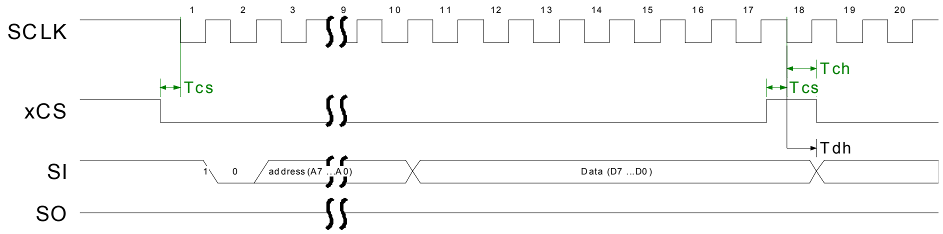

SCLK
1
2
3
9
10
11
12
13
14
15
16
17
18
19
20
Tch
Tcs
Tcs
xCS
Tdh
SI
1
0
address (A7 ...A0)
Data (D7 ...D0)
SO

Figure 1-8. Serial Interface Sequential Read

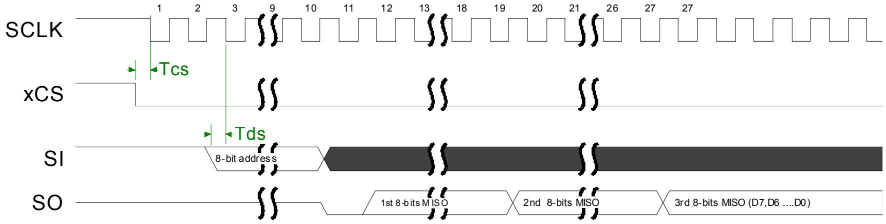
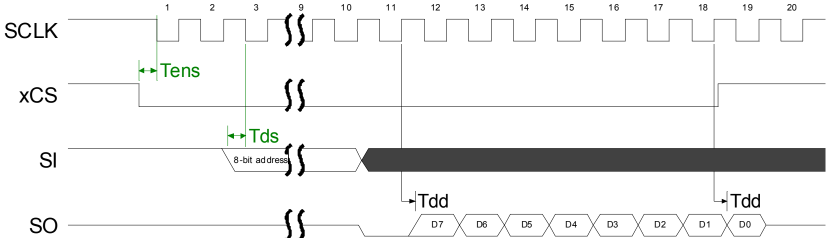

SCLK
1
2
3
9
10
11
12
13
18
19
20
21
26
27
27
Tcs
xCS
Tds
SI
8-bit address
SO
1st 8-bits MISO
2nd 8-bits MISO
3rd 8-bits MISO (D7,D6 ....D0)

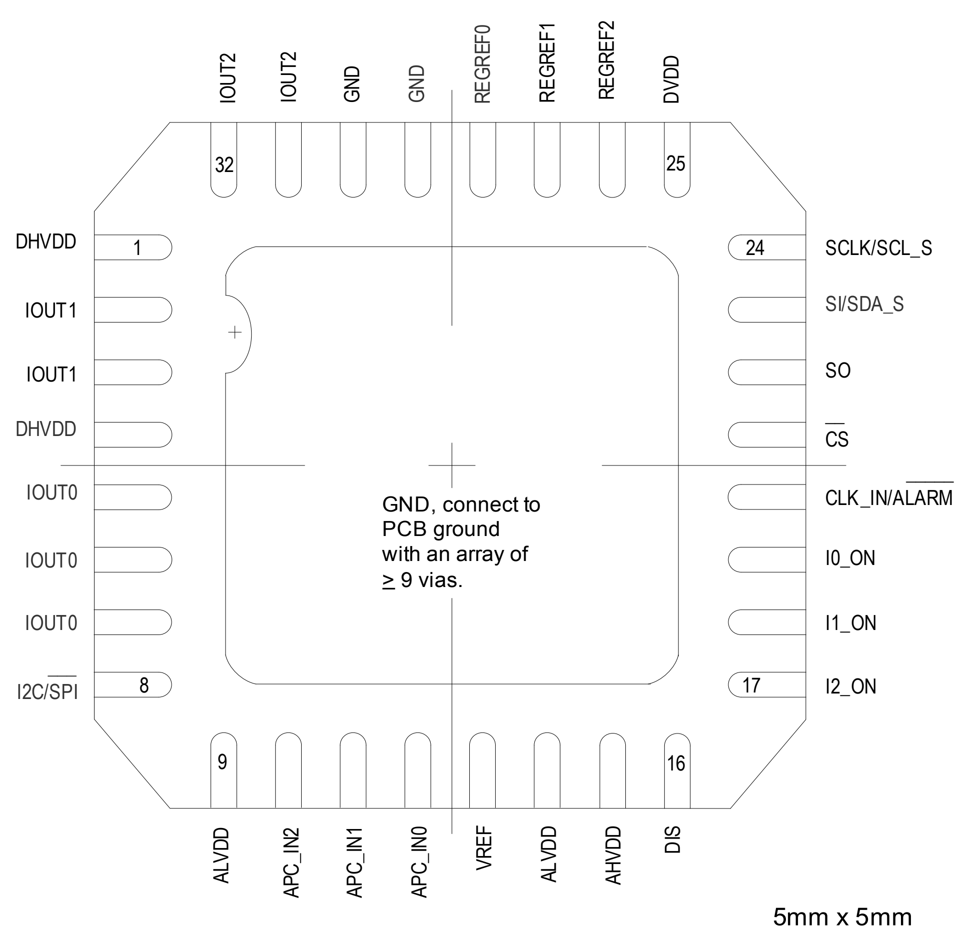
Figure 1-9. Serial Interface Random Read


SCLK
1
2
3
9
10
11
12
13
14
15
16
17
18
19
20
Tens
xCS
Tds
SI
8-bit address
Tdd
Tdd
SO
D7
D6
D5
D4
D3
D2
D1
D0

1.11 M08886 Pinout

The M08886 is packaged in a 5x5 mm 32-pin QFN package with 0.5 mm pin pitch.

Figure 1-10. M08886 Pinout


IOUT2
IOUT2
GND
GND
REGREF0
REGREF1
REGREF2
DVDD
32
25
DHVDD
1
IOUT1
IOUT1
DHVDD
IOUT0
IOUT0
IOUT0
I2C/SPI
8
24
SCLK/SCL_S
SI/SDA_S
SO
CS
CLK_IN/ALARM
I0_ON
I1_ON
17
I2_ON
GND, connect to
PCB ground
with an array of
≥ 9 vias.
9
16
ALVDD
APC_IN2
APC_IN1
APC_IN0
VREF
ALVDD
AHVDD
DIS
5mm x 5mm

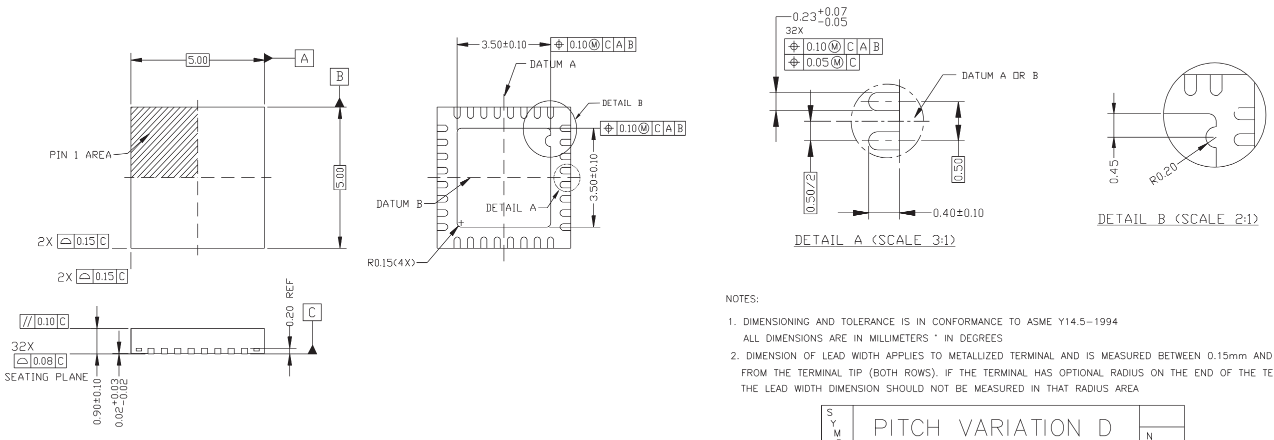
1.12 Pin List and Descriptions

Table 1-12. Pin List and Descriptions

Pin	Name	Type	Function
1 and 4	DHV_{DD}	Supply	3.3 V digital supply
2 and 3	IOUT1	Analog	1A LED/Laser driver output
5, 6 and 7	IOUT0	Analog	2A LED/Laser driver output
8	$I^2C/\overline{SPI}$	CMOS(PD)	Serial interface select (L=I^2C,H=SPI)
9 and 14	ALV_{DD}	Supply	1.8 V analog supply
10	APC_IN2	Analog	Monitor PD input 2 (assignable)
11	APC_IN1	Analog	Monitor PD input 1 (assignable)
12	APC_IN0	Analog	Monitor PD input 0 (assignable)
13	VREF	Analog	Current reference generator
15	AHV_{DD}	Supply	3.3 V analog supply
16	DIS	CMOS(PU)	Disable all laser drivers
17	I2_ON	CMOS(PD)	Turns on driver 2
18	I1_ON	CMOS(PD)	Turns on driver 1
19	I0_ON	CMOS(PD)	Turns on driver 0
20	CLK_IN/$\overline{ALARM}$	CMOS	External clock input or alarm output
21	$\overline{CS}$	Open Drain (PU)	Serial enable
22	SO	Open Drain (PU)	Serial data out
23	SI/SDA_S	Open Drain (PU)	Serial data in/I^2C data slave
24	SCLK/SCL_S	Open Drain (PU)	Serial clock/I^2C clock slave
25	DV_{DD}	Supply	1.8 V digital supply
26	REGREF2	Analog	Regulator reference output 2 (assignable)
27	REGREF1	Analog	Regulator reference output 1 (assignable)
28	REGREF0	Analog	Regulator reference output 0 (assignable)
29 and 30	GND	Supply	Ground
31 and 32	IOUT2	Analog	1A driver output
center pad	GND	Supply	Electrical and Thermal Ground (must be connected electrically)
NOTE: PD means pulled down, PU means pulled up.			

1.13 Package Information

Figure 1-11. Sawn QFN32 Package Information


5.00
A
B
PIN 1 AREA
5.00
2X ⌓ 0.15 C
2X ⌓ 0.15 C
// 0.10 C
32X
⌓ 0.08 C
SEATING PLANE
0.90±0.10
0.02+0.03 −0.02
0.20 REF
C
3.50±0.10
⌖ 0.10 Ⓜ C A B
DATUM A
DETAIL B
⌖ 0.10 Ⓜ C A B
3.50±0.10
DATUM B
DETAIL A
R0.15(4X)
0.23+0.07 −0.05
32X
⌖ 0.10 Ⓜ C A B
⌖ 0.05 Ⓜ C
DATUM A OR B
0.50/2
0.50
0.40±0.10
DETAIL A (SCALE 3:1)
0.45
R0.20
DETAIL B (SCALE 2:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5−1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	32			3
Nd	8			3
Ne	8			3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	3.15	3.30	3.45	
E2	3.15	3.30	3.45	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3	0.20 REF.			
D	5.00 BSC			
D1	4.75 BSC			
E	5.00 BSC			
E1	4.75 BSC			
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
△3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
△4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
△6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
△8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
△10. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
△11. APPLIED ONLY FOR TERMINALS.

2.0 Functional Description

The M08886 is a highly integrated laser/led driver for LCD/LCoS laser/led projection display applications. It provides control and monitoring of up to three LEDs/lasers (typically RGB: red, green and blue) and monitoring and control of temperature and DC-DC converters reference generators for optimal laser/led supply.

The RGB laser/led front end consists of three 12-bit current output digital to analog converters (DACs) and three high efficiency laser drivers with de-speckle technology. The current generated by each DAC is the sum of two components - an offset component (corresponding to the threshold current of the laser, set offset to 0 for LEDs) and a gain component corresponding to the video information.

During projection, the laser/LED current can be controlled by writing the desired current directly to the output DAC or the Laser/LED current can be controlled by an external photodetector. In this case ColorMinder Automatic Power control loop (APC) continually adjusts the gain component of the laser/led current to hold the photodiode current constant during its “on time” and therefore the optical power of the laser/led is held constant at the desired value. The APC will match the photodetector current corresponding to the laser/led turned on at that moment with the current programmed by the video processor for the 13bit target analog to digital converter as the target. The current generated by the target DAC corresponds therefore to the desired optical power level. The APC adjusts the laser/led drive currents in order to maintain the appropriate optical power. The optical power is adjusted every time a color is on during a frame or a portion of it. The threshold current for the lasers (offset portion of the DAC currents) are also automatically adjusted by the APC loop during the blanking period (*I0_ON, I1_ON* and *I2_ON* all low) or they can be programmed by the user.

The M08886 internally monitors the required laser/led driver headroom and sends a control signal to an external DC-DC converters to optimally adjust each laser/led’s supply voltage.

The M08886 internal registers are loaded from an external microcontroller through a slave I^{2}C interface or a 4-wire high speed interface. The host µcontroller can monitor and read back the analog to digital converter outputs either though the slave I^{2}C or the SPI interface.

2.1 Automatic Power Control (APC)

ColorMinder automatic power control (APC) can keep the laser/led power constant and the color balanced by comparing the monitor photodetector (RGB color sensor) currents to target values programmed into the 13-bit target DACs.

At power-up the APC can be enabled/disabled independently for each channel by setting apc**x**_ctrl0[2:1]=11. For channels with disabled APC the laser/led currents are controlled through the serial interface using bits iout**x**_gain[11:0].

It is possible to freeze the APC loop for each channel by using loop_ctrl[2:0]. In this case the M08886 will stop updating the gain or offset *IOUT**x*** currents independently of the state of *I**x**_ON* pins.

The photodiode (RGB sensor) target values are programmed via the serial interface in registers target2[12:0], target1[12:0] and target0[12:0] respectively for *IOUT2*, *IOUT1* and *IOUT0. When* the corresponding color is turned on as signaled by the transition of *I0_ON, I1_ON* or *I2_ON* from low to high the LED/Laser drive currents are automatically adjusted up or down to always make the photodetector current (RGB sensor current) match the target current.

If desired, these target currents can be adjusted on a frame by frame basis to optimize contrast and save battery power depending on the brightness required for a particular frame.

When an *I**x**_ON* signal is enabled (low to high transition) the new APC target is strobed in and the proper incoming monitor photodetector current is selected to control the output current by an analog multiplexer from *APC_IN0, APC_IN1 or APC_IN2.* For each output channel the photodetector input corresponding can be selected using apc**x**_ctrl0[2:1]. This allows the use of multiple independent photodetectors such as a 3 channel RGB color sensor with color filters optimized for each channel or instead a single broadband (color insensitive) photodetector can be used for all 3 channels. If a single broadband photodetector is used and connected to *APC_IN0* all the apc**x**_ctrl0[2:1] should be set to 00b.

2.1.1 Simple Implementation of APC Control

In addition to the controls described in this section, also see the section below on the TIA.

If the APC targets are not changing frame by frame, a basic register configuration can be used as shown below.

Table 2-1. Basic Register Configuration for APC Control

Name	Address	Recommend Setting	Description
loop_ctrl	0x29h	00h	
apc0_ctrl0[2:1] apc1_ctrl0[2:1] apc2_ctrl0[2:1]	0x40h[2:1] 0x3Ch[2:1] 0x38h[2:1]	00000xx0b 00000xx0b 00000xx0b	Select which photodiode (RGB sensor) input will control which output. Setting depends on hardware connection to photodiode(s) and which channels will use APC control. See Register description for details.
target**x**ith_msb target**x**ith_lsb	0x2Ch, 0x2Dh, 0x30h, 0x31h, 0x34h, 0x35h	00h	Set the laser offset (threshold) at 0. See section on Despeckle for use of laser offset.
target**x**_msb target**x**_lsb	0x2Ah, 0x2Eh, 0x32h 0x2Bh, 0x2Fh, 0x33h	000xxxxxb xxh	Set the gain target at desired level
apc0_ctrl2 apc1_ctrl2 apc2_ctrl2	0x3Eh 0x3Ah 0x36h	00h	Set the clock step to 0 for controlling the step response of the output
apc0_ctrl1 apc1_ctrl1 apc2_ctrl1	0x3Fh 0x3Bh 0x37h	03h	Clock divide set to 16.

The APC controller increases or decreases the value of the gain portion of the laser/led *IOUT**X*** current so the photodetector current will match the gain target current for that channel.

If more than one laser/led is turned on (2 or 3 of *I0_ON*, *I1_ON* or *I2_ON* are high at the same time) the M08886 freezes the update of the APC loop for as long as more then one of the *I**x**_ON* signal is on. This prevents the APC loop from using wrong photodetector information in case a single photodetector is used with no color filter. It should be noted that 2 or more low to high transitions of any of the *I0_ON, I1_ON* or *I2_ON* within 200 ns of each other will violate internal timing and will result in unpredictable operation. Care should be taken to prevent damage to the part when multiple laser/leds are enabled. The power dissipation of the part should be kept below the level that will result in a die temperature exceeding 125 °C.

2.1.2 Highly Featured Implementation of APC Control

Table 2-2. Highly Featured Register Configuration for APC Control

Name	Address	Recommend Setting	Description
loop_ctrl	0x29h	00h	Setting 0x29h[7:5]=111b may be useful for very low EMI applications with slow current slew on the outputs. Set 0x29h[3]=1b when using an external clock in PWM or MPG mode.
apc0_ctrl0[2:1] apc1_ctrl0[2:1] apc2_ctrl0[2:1]	0x40h[2:1] 0x3Ch[2:1] 0x38h[2:1]	00000xx0b 00000xx0b 00000xx0b	Select which photodiode (RGB sensor) input will control which output. Setting depends on hardware connection to photodiode(s) and which channels will use APC control. See Register description for details.
target**x**ith_msb target**x**ith_lsb	0x2Ch, 0x2Dh, 0x30h, 0x31h, 0x34h, 0x35h	00h	Set the laser offset (threshold) at 0. See section on Despeckle for use of laser offset.
target**x**_msb target**x**_lsb	0x2Ah, 0x2Eh, 0x32h 0x2Bh, 0x2Fh, 0x33h	000xxxxxb xxh	Set the gain target at desired level
apc0_ctrl2 apc1_ctrl2 apc2_ctrl2	0x3Eh 0x3Ah 0x36h	A8h	This setting may vary depending on photodiode capacitance, desired risetime and how much overshoot can be tolerated.
apc0_ctrl1 apc1_ctrl1 apc2_ctrl1	0x3Fh 0x3Bh 0x37h	92h	This setting may vary depending on photodiode capacitance, desired risetime and how much overshoot can be tolerated

One of the reasons to choose a more complicated APC control method is modulation of frame-to-frame illumination. Modulating the output amplitude of the Laser/LED can increase the contrast in an image and it can improve battery life. Changes in the LED/Laser output on a frame-by frame basis requires that the LED/Laser “step” to the new APC target amplitude in a fraction of the frame time. The fast step to a new level requires that some care be taken in the feedback response of the photodetector and LED/Laser.

Other reasons to choose a more complicated APC control method might be slew rate control of the outputs for EMI or DC-DC converter stability reasons. In this case the feedback response does not require as much consideration.

The primary methods for adjusting the feedback response of the photodetector are in registers apc**x**_ctrl2,1,0. The TIA response will also need to be compensated as described in the section below.

The digital APC loop is designed to settle to the desired optical output power in 5 µs: the optical power measured in the subsequent 5 µs should be within +/-1% of the desired value. To achieve optimal settling time, the APC loop must be adjusted to the laser/led/monitor photodetector characteristics.

Each *IOUT**X*** slew rate is independently controllable in 3 time intervals. The first time interval begins when *I**x**_ON* goes high and the length of the first time interval is defined in apc**x**_ctrl2[7:6] and is from 0 to 255 clock cycles. The length of the second time interval is defined in apc**x**_ctrl2[5:4] and is from 0 to 127 clock cycles. The length of the third time interval is defined in apc**x**_ctrl2[3:2] and is from 0 to 127 clock cycles. There is a fourth time interval which is not definable which is from the end of the third time interval until the time when *I**x**_ON* goes low.

The APC clock is the system clock divided by 3. The PWM and MPG clock is the system clock divided by 16 and may be further divided by register clk_div[7:0]. The source of the system clock is set in register despeckle_clk[1:0]. If only LED light sources are used (despeckle for lasers not needed) then power consumption can be minimized by selecting despeckle_clk[1:0]=11b and osc_ctrl[3]=1b. If the despeckle feature is used then despeckle_clk[1:0]=00b and osc_ctrl[3]=0b and the clock frequency can be tuned at osc_ctrl[2:0]. The APC clock for each channel may be divided (apc**x**_ctrl1[1:0]) and the point at which the clock division begins following *I**x**_ON* high (apc**x**_ctrl2[1:0]) can also be set. So a clock cycle in an early interval may be different than a clock cycle in a later interval. And the change in clock rate may occur in the middle of an interval. Decimation may also be enabled for any of the APC channels at apc**x**_ctrl0[7:5]. If decimation is enabled then the APC loop will not correct the output current until the measured photodiode current doesn't match the target photodiode current several measurements in a row with the same polarity (too high or too low). The number of consecutive measurements required of the same polarity is determined by the decimation factor.

During the first time interval following I***x**_ON h*igh the corresponding *IOUT**X*** output current will increase by an amount defined in apc**x**_ctrl1[7:6] each clock cycle if the photodetector current is less than the target current set in target**x**_msb and target**x**_lsb and it will decrease by that amount each clock cycle that the photodetector current is less than the target current. Similarly during the second time interval the *IOUT**X*** output current will increase/decrease by an amount defined in apc**x**_ctrl1[5:4] each clock cycle if the photodetector current is less/greater than the target current. During the third and fourth intervals the step size is always one LSB.

The *OUT0* LSB is nominally 488 µA. The *OUT1* and *OUT2* LSBs are nominally 244 µA.

The overshoot of the *OUT**X*** output current will be at a maximum during the first time interval where the current step is greatest. It will be proportional to the current defined in apc**x**_ctrl1[7:6] and it will also be a function of the loop delay which is approximately 3 clock cycles. Either an over-damped or under-damped response may independently be programmed into the response of the M08886 output channels as desired.

The target DAC has a conversion rate of 30 MSPS and the full scale value is 3 mA with a resolution of 13 bit or 0.366 µA. As an example, if the full scale photodetector value is 200 µA, the possible selectable power levels are up to 546 decimal (200 µA /0.366 µA). In this example, full scale will correspond to a target DAC (target**x**[12:0]) value of 111h and no power will correspond to 0h.

2.1.3 Compensating the TIA at the Photodetector Input

The maximum photodetector current supported by the M08886 is 3 mA. Because of the different characteristics of each photodetector/laser/led the user should select the proper analog filter network for each of the channels by programming tia_ctrl[1:0].

2.1.4 Laser Offset (threshold) Tracking with APC

If lasers are being used instead of LEDs, the M08886 has the capability to automatically adjust offset (laser threshold) as well as gain. In most cases it is sufficient to only use the gain portion of APC control with a laser and the offset controls can be ignored. If the despeckle function is being used, offset tracking is a useful option.

The offset portion of the DAC currents is adjusted during the blanking signal following the period where the laser is on. The blanking period is automatically recognized by the M08886 as the period during which all the colors are off (*I0_ON, I1_ON* and *I2_ON* are all low). During that period the target DAC is switched to the user programmed target for the offset current and the M08886 will output and adjust only the offset (laser threshold) portion of the DAC, each of the 3 laser drivers will output only the current corresponding to the threshold (offset DAC current) and the automatic power control loop will adjust the threshold during that period. The offset target for each of the lasers can be programmed using following registers target2_ith[12:0], target1_ith[12:0] and target0_ith[12:0]. The offset target should be chosen low enough as to not interfere with the blanking and high enough to allow meaningful feedback for the APC loop.

The decimation factor for offset control is set in register dec_off_ctrl[2:0]. The offset current will not be corrected until multiple occurrences of offset error are detected with the same polarity (too high or too low). The number of consecutive errors required before a correction is made is determined by the decimation factor.

During each blanking period the M08886 current starts from the previously determined and stored laser offset current. The laser driver will be able to track laser threshold variation even for short blanking periods because laser threshold varies slowly (typically based on temperature variation and laser aging). The minimum allowed blanking signal is 200 nsec.

Laser threshold tracking by means of APC can be disabled individually at power-up for each channel using apc**x**_ctrl0[4] and it is automatically disabled if apc**x**_ctrl0[2:1]=11b (APC disabled). The threshold current can be programmed in the part for each of the lasers using bits iout**x**_offset[11:0]. If the programmed offset current does not track (with temperature and laser aging) the actual laser offset, the APC settling might be slowed down or laser power overshoot at turn-on might occur. When the APC for the offset current is disabled the part will automatically output 0 current for all the lasers during blanking.

2.2 LASER/LED Current DACs

The M08886 includes three monotonic digital to analog converters (DACs) which generate the currents for the three laser/leds, the current is converted from a digital code given by the sum of the offset (laser threshold) and gain (video information). The offset and gain values can be either updated via registers or by the APC loop as described in the previous paragraph.

The three laser/led DACs have a range scaled to the laser/led driver output of 0 to 1A for *IOUT1* and *IOUT2* and 0 to 2A for *IOUT0*, a resolution of 12 bits and an update rate of 30 MSPS.

The integrated laser/led drivers deliver the DACs current to the laser/led diodes.

The drivers include MACOM proprietary de-speckle feature which significantly reduces appearance of speckle in laser light by means of high speed modulation of the laser driver current. The de-speckle feature can be simply enabled or disabled via register despeckle_ctrl[7:0]. With the APC loop enabled, the M08886 automatically adjusts the power level and no other adjustments are required. If open loop is used then laser power calibration must be performed with the de-speckle feature enabled.

Each laser/led driver output (*IOUT***x**) is controlled by the corresponding ON signal (*I***x**_*ON*). Rise/fall time from the laser/led driver is typically 2 ns into a resistive electrical load. The risetime will be dominated by the DC-DC converter settling time in applications where a single DC-DC converter output voltage tracks the optimal LED/laser anode voltage.

To match the significantly slower rise and fall time of the LCD/LCoS the M08886 features a programmable delay which can shift the turn-on of the laser/led once the corresponding ON signal goes to high. The delay is implemented as a programmable 10bit counter that counts clock cycles of the internal clock selected at register 0x28h[1:0] divided by 16. (either 320 MHz or 42 MHz may be selected). If the 320 MHz/16 oscillator is selected then 19.5 MHz clock cycles are counted at the rising edge of each laser/led ON signal (*I0_ON, I1_ON* and *I2_ON*) the counter is decremented and the laser/led is actually turned on only when the counter reaches 0. The laser/led is turned off on the falling edge of the corresponding laser/led ON signal (*I0_ON, I1_ON, I2_ON*). The maximum delay achievable is therefore 52.4 µs if the 320 MHz/16 clock is selected (1023 times the 50 ns period of the 19.5 MHz internal oscillator). Additional delay can be achieved by using the M08886 programmable divider of the internal clock. The internal clock can be divided down by a factor of 1, 2, 4, 16, 256, 512, 1024, and 2048. This can be obtained by writing register clk_div[7:4]. The values of the programmable counter for the red, green and blue laser/led are stored in bits on_count2[9:0], on_count1[9:0], and on_count0[9:0] respectively. The rising edge of the *I***x**_*ON* signals strobe the corresponding on_count**x**[9:0] value into the M08886 timing controller therefore if the on_count register value is changed during the on time for that color the effect of the register change will be available during the next color cycle.

If the on_count**x** is programmed to 00 0000 0000b the PWM feature is disabled for *IOUT***x**.

2.2.1 Increasing the Maximum LED/Drive Current by Combining Outputs

When multiple channels (2 or 3) of the M8886 inputs and outputs are shorted together to obtain a single higher current channel then set opmode_ctrl0[5]=1b. The Ix_ON should be shorted together for the channels that are being combined and if they are not shorted their state changes should occur within 10 ns of each other.

It should be pointed out that the M08886 has a single bias generating circuit which is toggled between different output stages depending on the Ix_ON.

The architecture is such that, when multiple outputs are enabled, the biasing is generated from one of them (the one with the lowest channel number) and fed to the other channel. Because of typical circuit fabrication variations and mismatches the current out of a certain channel may therefore vary between the case when the channel is operated independently vs. the case when channel is operated in conjunction with another as when a channel is operated independently the biasing is generated by its own biasing circuit. This does not impact the current stability over supply and temperature of the current generated by each channel.

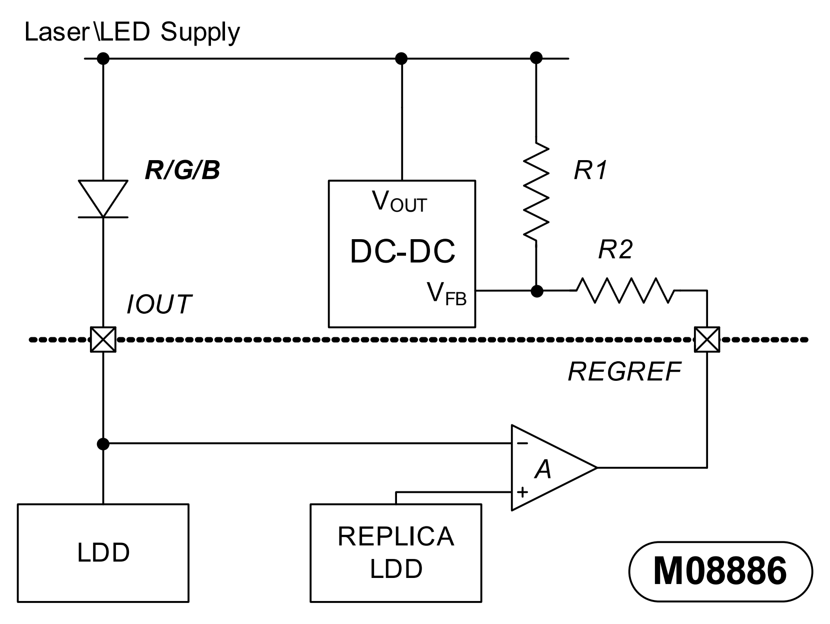
For example, if channel 0 and channel 1 are shorted at the input and output the biasing for channel 1 is now controlled by channel 0.

2.3 Laser\LED Voltage Supply Control

By controlling the Laser\LED anode voltage with the REGREF outputs the M08886 can optimize (minimize) the voltage on the output drive pins to the level that insures accurate current drive levels and minimizes power dissipation. Nominally the outputs need 350 mV of headroom but the M08886 will determine the actual level. An internal amplifier is used to monitor the output stage voltage drop and to compare it against an internal reference voltage coming from a replica circuit. The output of the amplifier at the REGREF pins will control the feedback input of a DC-DC converter to adjust the output voltage (LED or Laser anode voltage) of the DC-DC converter.

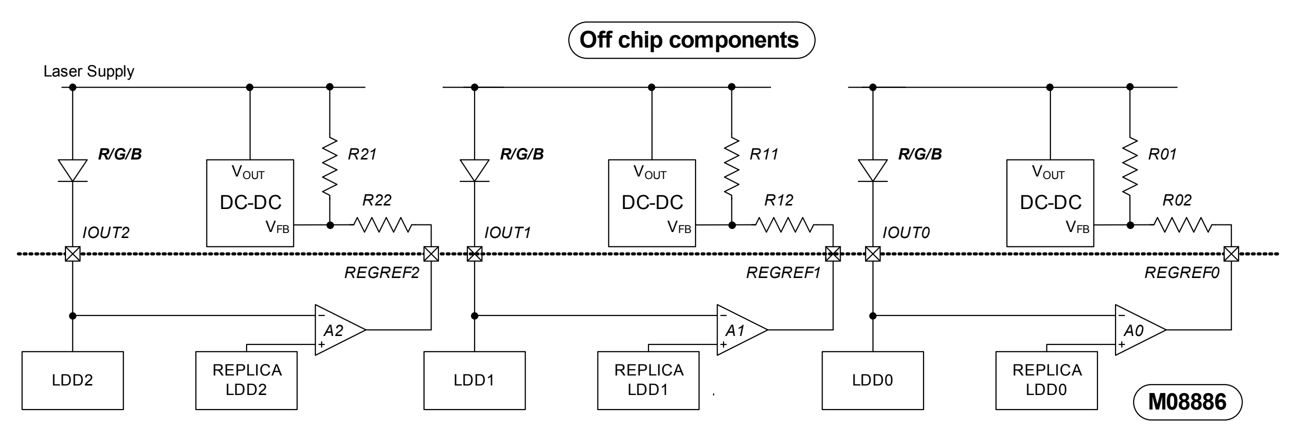
The block diagram below illustrates the use of this feature in the system.

Figure 2-1. laser/led Supply Control Block Diagram


Laser\LED Supply
R/G/B
IOUT
VOUT
DC-DC
VFB
R1
R2
REGREF
A
LDD
REPLICA LDD
M08886

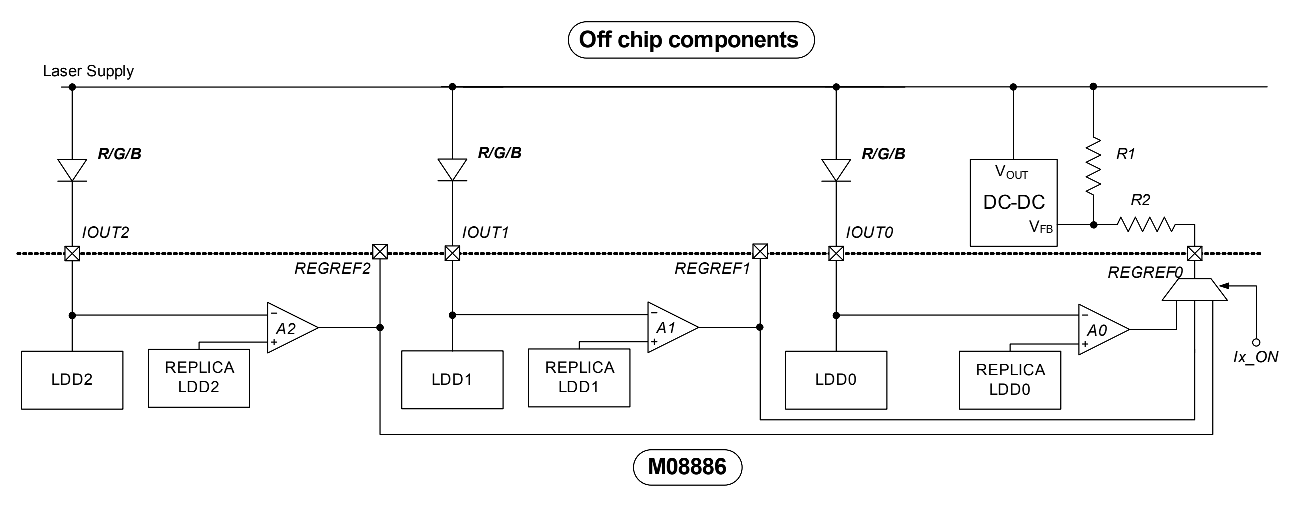
In fact there are three laser/leds and therefore three channels in the REGREF. The following block diagram shows the three channels together.

Figure 2-2. Controlling Laser/LED Supply with Three DC-DC Converters


Off chip components
Laser Supply
R/G/B
VOUT
DC-DC
VFB
R21
R22
IOUT2
REGREF2
A2
LDD2
REPLICA LDD2
R/G/B
R11
R12
IOUT1
REGREF1
A1
LDD1
REPLICA LDD1
R/G/B
R01
R02
IOUT0
REGREF0
A0
LDD0
REPLICA LDD0
M08886

In case a single DC-DC converter is used, *REGREF0* can be multiplexed automatically between three output values. The following block diagram shows this configuration. The strobe signal for each of the three pre-programmed output of *headroom setting DAC* can be independently programmed to be the falling or raising edge of the *I**x**_ON* signals. This feature allows a single DC-DC converter to be used to generate the supply for all the laser/leds independently of the order of color cycling in the projector system. When the falling edge is selected, one of the two possible color sequence needs to be selected by using opmode_ctrl1[5].

Figure 2-3. Controlling Laser/LED Supply with Single DC-DC Converter



The M08886 internal circuitry will regulate the voltage at each of the *IOUT**x*** pins during the operation of the laser/led to a voltage equal to the required headroom of the laser/led driver in the actual operating condition by mean of adjusting the external DC-DC converter feedback point or reference voltage.

The replica circuit can be programmed to be a fixed 250 mV instead of the actual replica voltage, using out_ctrl**x** [7].

It should be noticed that the laser/led drop will depend on the intrinsic drop across the laser/leds (Vth) plus any drop caused by the series resistance, this includes the laser/led series resistance plus routing resistance on board and in the laser/led package, therefore the voltage drop across the laser/led needs to be adjusted under actual load conditions. This can be done for each *IOUT**x*** through bits out_ctrl**x** [6:4] regardless of the fact that the actual replica is used or the 250 mV fixed voltage.

To guarantee proper operation of the laser/led driver the loop controlling the laser/led supply should be faster then the required APC settling time. The overall supply control loop includes the M08886 and the DC-DC converter. The M08886 supply control path has a first pole at 30 MHz assuming a 5 pF load which should allow the loop to be stable assuming the DC-DC converter has a response time of tens of μs or faster. The load on *REGREF**x*** pins has a major effect on the internal circuitry of the part and care should be taken to minimize the loading and noise injection at this pin. For added flexibility and to help stability for different DC-DC converters, the gain of the difference amplifier can be programmed for each channel by means of regref**x**_ctrl[4:2].

In case a single DC-DC converter is used, *REGREF0* can be multiplexed automatically between three output values. The strobe signal for each of the three pre-programmed output of *headroom setting DAC* can be independently programmed to be the falling or raising edge of the *I**x**_ON* signals. This feature allows a single DC-

DC converter to be used to generate the supply for all the laser/leds independently of the order of color cycling in the projector system. When the falling edge is selected, one of the two possible color sequence needs to be selected by using opmode_ctrl1[5].

In order to protect the high speed circuitry of the laser/led driver from the high voltage supply at the anodes of the laser/leds, it is imperative that a small quantity of current flow through the laser/led so that the laser/led forward voltage lowers the voltage at the M08886 output pin. The voltage at the laser/led driver output should never exceed 3.63 V therefore an external resistor should be added between the laser/led cathode and ground. The value of the resistor should be chosen so the current flowing is enough to create a sufficient voltage drop on the laser/led. The APC loop will automatically compensate for this “off” current. If the APC loop is disabled and the M08886 is operated open loop this current should be accounted for when programming the desired currents in the system calibration phase. When a single DC-DC converter is used, care should be taken to guarantee that the voltage drop across the red and green laser/led is such that, when the supply is regulated for operation with the highest voltage laser/led, the voltage at all driver pins never exceeds 3.63 V.

Alternative methods to protect the output pins might include a schottky diode to the 3.3 V supply or very low voltage zener.

2.4 Pulse Width Modulation (PWM)

The high divider ratios of the internal clock divider (256, 512, 1024, 2048) in conjunction with the programmable counter can be used to decrease the amount of time each laser is on. The optical power can then be controlled by modulating the pulse width of each color pulse. This can yield substantial power savings in laser applications.

The internal ring oscillator varies by +/-15% over parts, temperature and supply and this can directly translate into color intensity variation. The M08886 features a clock input where a high precision clock can be fed to the part and used for this power saving feature. A common 19.44 MHz crystal oscillator or a resonator can be used for this purpose or any high precision clock already available in the system. The precision of PWM power control is directly proportional to the clock accuracy. The PWM block is designed to operate with a maximum frequency of 25 MHz. If CLK_IN is higher then 25 MHz then the CLK_IN divider should be enabled and set to 2 or 4 at register clk_ctrl[2:1] to appropriately scale the frequency. A maximum external clock of 100 MHz is allowed but the internal PWM block can operate at a maximum speed of 25 MHz. External clocks of less than 19.44 MHz are also allowed. The PWM generator then will work at the speed of the *CLK_IN* (assuming no divider is enabled). The external clock can be selected with register loop_ctrl[3].

Table 2-3. Clock Selection for PWM and MPG

	Register Setting	Description
Laser Mode	0x28h[1:0]=00b	320 MHz system clock selected. PWM and MPG clock is this clock divided by 16
LED Mode	0x28h[1:0]=11b	42 MHz system clock selected PWM and MPG clock is this clock divided by 16

2.5 Multi Pulse Generator (MPG)

The M08886 allows for the drive of any of the laser/leds by means of multiple pulses. The multi-pulse generator (MPG) operates in a manner similar to the PWM generator. For each of the laser/leds, two 10-bit counters specify the number of internal clock cycles during which the laser/led associated with them is kept on (gain plus offset current) and off (0 current). Similar to the PWM block, the MPG block can also use an external clock signal (*CLK_IN*).

Assuming the 320 MHz/16 internal oscillator is used, the duty cycle of the pulsed waveform can be controlled with a resolution of one 19.5 MHz clock period or 51.28 ns. If both counters are loaded with the maximum value (1023) the signal driving the laser/led will be a square wave of period 102 µs (9.775 kHz). If an external clock is supplied the maximum resolution achievable is 40 ns (25 MHz clock).

The MPG clock can be divided by a factor of 1, 2, 4, 16, 256, 512, 1024, and 2048. This can be obtained by writing register clk_div[3:0]. Register clk_div[3:0] is independent of the divider ratio used in the PWM mode (clk_div[7:4]).

In general the maximum obtainable period for the multi-pulse waveform is 2046 times the clock period (2 times 1023 times the clock period), in this case the duty cycle of the multi-pulse waveform will be 50%.

Because of the 10-bit counter, the duty cycle resolution obtainable is 1/1023 or better then 0.1% assuming the highest count value is used for one of the counters. The duty cycle control resolution is inversely proportional to the maximum counter value.

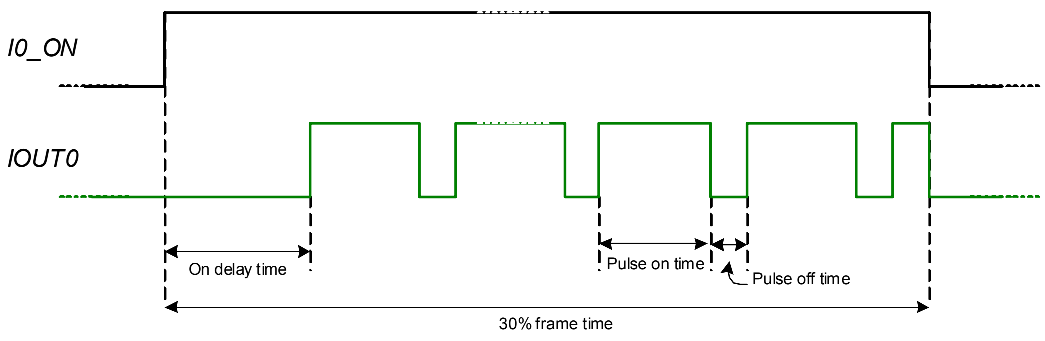
The control for the *IOUT0, IOUT1, IOUT2* laser/led on pulses are programmed respectively in the following registers: pulse_on2[9:0], pulse_on1[9:0] and pulse_on0[9:0].

The rising edge of the ***I*****x***_ON* signals strobe the corresponding pulse_on/off**x**[9:0] values into the M08886 timing controller. If the pulse_on/pulse_off register value is changed during the on time for that color the effect of the register change will not occur until the next rising edge of that ***I*****x***_ON*.

If the pulse_on or pulse_off for a channel is programmed to 000h then the MPG function is disabled for that channel.

The MPG function is independent of the PWM function: the “On delay time” (PWM function), the “Pulse on time” and “Pulse off time” (MPG functions) can be programmed independently. Also the clock divider for the “On delay time” the “Pulse on/off time” can be selected independently allowing flexibility in defining the driving signals. This is illustrated by the following diagram, where an example for the green laser assigned to channel 0 is represented: the green on signal (*I0_ON*) and laser current output (*IOUT0*) are drawn.

Figure 2-4. Multi Pulse Generator Timing



2.6 Power Save Features

Both the APC and the PWM features can be used to obtain significant system power savings.

The capability of M08886 APC to adjust the laser/led outputs frame by frame allows for significant power savings compared to leaving the laser/leds on all the time at full power. If frame by frame APC is used, then the external µcontroller will store a new 2 byte value in the target DAC for the next power level for each color power that is changing prior to displaying the new frame.

PWM mode also leads to significant power reduction versus standard amplitude modulation. With PWM mode before the display of every new frame the external µcontroller should specify for each color the delay required for pulse width modulation by programming the counter of each color. This can be done by writing four 8-bit registers.

Both power saving methods can be used simultaneously (on different color sources) to obtain the maximum power savings and control over color content of each frame.

The MPG block can also be used as a power saving feature where the color intensity is modulated by varying the duty cycle of the pulsed waveform. In this case the pulse_on/off registers for every laser need to be programmed to the value corresponding to that frame for a total of eight 8-bit register writes for each new frame. When using MPG with duty cycle modulation for power save mode, accurate power control can be achieved without the use of external clock because internal oscillator variations affect both the on and off period hence the ratio between on/off time remains constant. However, if a very limited number of multiple pulses are used during a frame the internal oscillator variations might impact laser power accuracy.

2.7 Safety

A disable pin (*DIS*) is available on the M08886. It disconnects the laser/LED path to ground within 1 µs of a low to high transition of *DIS* the laser/led driver current is reduced to 1/10th of its starting value.

A register alarm is also available: the safety monitor block compares the output current of each laser/led with 3 thresholds (one for each of the laser/leds) and an alarm is issued if the current is higher than the programmed threshold for any of the lasers/LEDs. The digital thresholds can be programmed in the following registers: alarm_th**x**[7:0], these values will be compared to the MSB of the output current.

If C*LK_IN* is not being used by MPG or PWM then the pin can be used as an alarm output and external circuitry can be used to shut down power to the laser/leds. Or the alarm status may be read back from register alarm[7:0]. Register Alarm[7:0] is not self clearing: once an alarm has occurred, it must be cleared by the user by writing a 1 to strbalrm_ctrl[0].

The M08886 can also be programmed (opmode_ctrl1[3]) to automatically disable the laser/LED outputs when the drive current exceeds the programmed threshold. In this case the laser/led current for that particular laser/led is automatically forced to 0. This feature can be disabled via registers.

The *ALARM* pin is an open collector output and can operate in status mode or interrupt mode. This can be selected at register opmode_ctrl0[3]. In status mode the alarm is provided directly to the pin and the pin will be asserted as long as the alarm is present. In some cases the alarm may only be present for only one clock cycle of the internal high speed clock. If the external load on *ALARM* pin is excessive the alarm signal may not appear at the output because one clock cycle is only 10 ns (100 MHz clock). In interrupt mode the M08886 will issue a positive going pulse on the alarm pin every time the internal alarm changes state. The width of the alarm pulse can be programmed at register opmode_ctrl0[3:0].

The output stage can also be disabled by the user at register opmode_ctrl1[1:0].

2.8 Programmable Serial Interface

The M08886 can be configured to use a 4-wire high speed serial interface or I^2C. This can be achieved by connecting pin *SerSel* high or low respectively.

When the part is configured to use I^2C an external host µController can access the register and read-back ADC codes from the slave I^2C (*SDA_S/SCL_S*). The maximum SCL_S clock rate is 3.4 MHz. 4.7 kΩ pull up resistors should be used at *SDA_S/SCL_S*. These pins are referenced to 1.8 V inside the M08886 but it is OK to connect the pull-up resistors to voltages as high as 2.5 V.

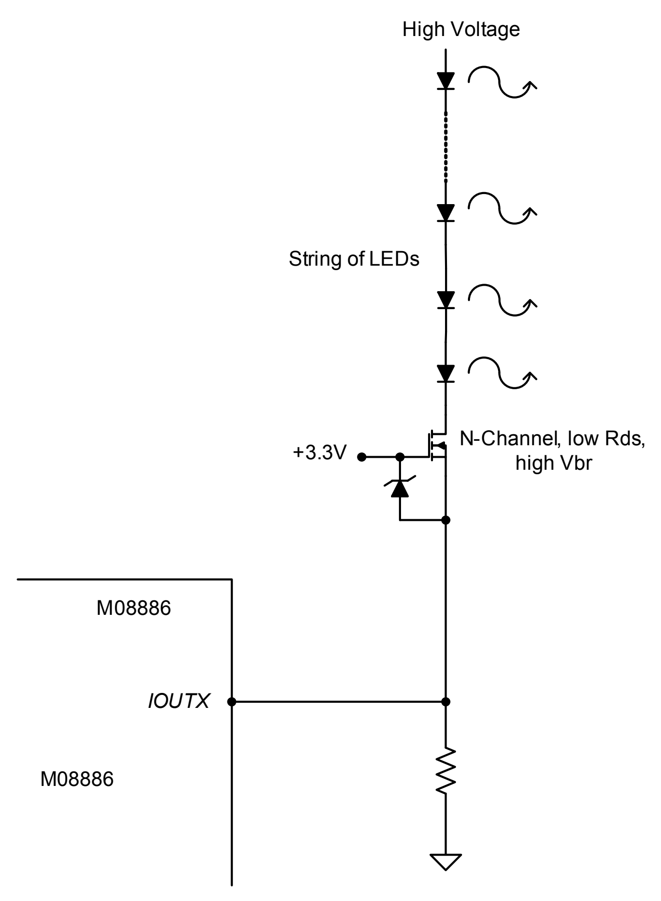
The I^2C slave address of the M08886 is fixed at 9Ch/9Dh.

The 4-wire high speed interface (*SCLC/SI/SO/*$\overline{CS}$) supports 40 MHz serial clock speeds.

2.9 Driving a String of LEDs from a High Voltage Supply

An M08886 can be used to drive a string of LEDs as shown in Figure 2-5 below. The M08886 must be isolated from the high voltage by an NFET transistor. The NFET should have a breakdown voltage greater than the high voltage supply and should also have a very low on resistance at 2.5 V gate-source voltage. The Diodes Inc. DMN2075U is an example of a suitable 20 V NFET.

Figure 2-5. Driving a String of LEDs from a High Voltage Supply


High Voltage
String of LEDs
+3.3V
N-Channel, low Rds,
high Vbr
M08886
IOUTX
M08886

2.10 Power Sequencing

Very high speed transistors are used on the M08886 outputs to achieve high efficiency and high performance (low voltage operation and high edge rate). These devices can withstand a maximum voltage of 3.3 V and it is necessary to protect them from the high voltages on the laser/led anodes. Internal protection diodes connect the outputs to the voltage supplies. To obtain reliable operation from the M08886 the power-up and power-down sequencing described in the diagrams below must be followed.

Figure 2-6. Power-Up

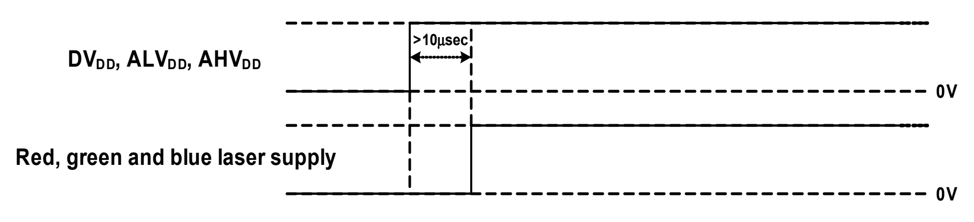
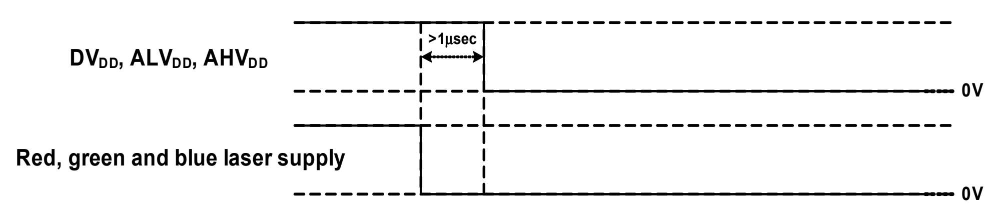

DV_{DD}, ALV_{DD}, AHV_{DD}
>10µsec
0V
Red, green and blue laser supply
0V

Figure 2-7. Power-Down


DV_{DD}, ALV_{DD}, AHV_{DD}
>1µsec
0V
Red, green and blue laser supply
0V

2.11 Layout Considerations

The center pad of the package is the electrical ground and the heat sinking path for the M08886. The center pad should be connected to an internal ground plane through an array of 9 or more vias.

The accuracy of the internal DACs and the LED/laser drive amplitudes and timing depend on pin VREF being noise-free. The resistor at this pin should be close to the M08886 and the via to ground from the resistor should be nearby.

The external DC-DC converter will amplify any noise on the REGREF pins. Care should be taken in routing these pins so they are not parallel to the laser/LED drive signals or clock signals.

Decoupling capacitors should be on the same side of the PCB as the M08886 and close to the pin they are decoupling. Vias to ground and voltage supplies should not be shared by components or signals (crosstalk between signals will occur).

3.0 Registers

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
General REGISTERS											
00h	opmode_ctrl0	i_fullscale	pd_trgetDAC	en_IO	RSVD	alrm_ctrl<3:0>				00001000	R/W
		Sets current full scale: 1: 75% 0: 100%	Powers down target DAC: 1: powers down target DAC (Open Loop mode) 0: normal operation (APC active)	1: Enable parallel input 0: normal operation		Controls the behavior of the $\overline{\text{ALARM}}$ 1xxx: Status mode 0000: Interrupt mode with 1 cycle pulse width (1cycle=20 ns) 0001: Interrupt mode with 2 cycle pulse width 0010: Interrupt mode with 4 cycle pulse width …. 0111: Interrupt mode with 128 cycle pulse width					
01h	opmode_ctrl1	reg_num	edge	seq	Reserved	alarm_dis	Reserved	Soft Disable	DIS_bypass	00000000	R/W
		Number of DC/DC converters: 1: 1 0: 3	Switch regref output on: 1: Ix_ON falling edge 0: Ix_ON rising edge	Color sequence selector in case of falling edge: 1: 2-1-0 0:2-0-1	Reserved	Disable output on alarm: 1: disable output current on alarm 0: do not disable	Reserved	1: IOUTx disabled 0: IOUTx enabled	1: DIS pin ignored 0: DIS pin active		
02h	osc_ctrl	Reserved				osc_pd	osc_tune[2:0]			00000000	R/W
						1: Power down oscillator 0: Normal operation	Tune despeckle oscillator frequency 000b: 400 MHz 100b: 320 MHz (recommended) 111b: 270 MHz				
03h	clk_ctrl	clk_delay				alarm_clkin	clkin_div[1:0]		duty_en	00000000	R/W
		Input clock programmable delay: 0000 = no delay 0001 = 500nsec 0010 = 1000nsec … 1111 = 7500nsec				1: Pin 20 is $\overline{\text{ALARM}}$ 0: Pin 20 is CLK_IN	CLK_IN input clock divider: 00: 1 01: 2 10: 4 11: 3		1: enable duty cycle contro (Line mode control)l 0: disable duty cycle control (recommended for other modes)		
04h	reserved	RSVD								00000000	R/W

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
05h	out_ctrl2	rep_sel2_cc	offset_reg0[2:0]			snubber[2:0]			pd_iout2	00000000	R/W
		Selects replica voltage or constant voltage 0: replica 1: constant 250 mV	Adjust replica offset for IOUT2 000: 0 mV 001: 28.5 mV 010: 57 mV … 111: 200 mV			Control snubber network for IOUT2 (for use with despeckle to optimize the step response)			Master IOUT2 power down: 1: power down 0: enabled		
06h	out_ctrl1	rep_sel1	offset_reg1[2:0]			snubber[2:0]			pd_iout1	00000000	R/W
		Selects replica voltage or constant voltage 0: replica 1: constant 250 mV	Adjust replica offset for IOUT1 000: 0 mV 001: 28.5 mV 010: 57 mV … 111: 200 mV			Control snubber network for IOUT1 (for use with despeckle to optimize the step response)			Master IOUT1 power down: 1: power down 0: enabled		
07h	out_ctrl0	rep_sel0	offset_reg0[2:0]			snubber[2:0]			pd_iout0	00000000	R/W
		Selects replica voltage or constant voltage 0: replica 1: constant 250 mV	Adjust replica offset for IOUT0 000: 0 mV 001: 28.5 mV 010: 57 mV … 111: 200 mV			Control snubber network for IOUT0 (for use with despeckle to optimize the step response)			Master IOUT0 power down: 1: power down 0: enabled		
08h	reserved	Reserved								00000000	R/W
09h	regref2_ctrl	enpd_rep2	rep_pd_pol	hi_z	gm_tail	gain[1:0]		pol_swap	pd regref2	00000000	R/W
		Power down IOUT2 replica when I2_ON is off (other channel 2 settings may affect replica power down timing) 0: no power down 1: powered down	Voltage at REGREF2 when replica is powered down 0: 0 V 1: AHVDD	REGREF2 outputstate. This bit will only affect REGREF2 if 0x09h[0]=1 **1:** REGREF2 is high impedance **0:** 0x09h[6] determines state	1: Reduces tail current (gain is reduced to 0.6x) 0: Normal operation Loop gain adjustment of DC-DC converter	00: 70 01: 32 10: 15 11: 7		Select gm call polarity 1: normal 0: swapped	power down REGREF2 1: power down 0: normal operation		

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
0Ah	regref1_ctrl	enpd_rep1	rep_pd_pol	hi_z	gm_tail	gain[1:0]		pol_swap	pd_regref1	00000000	R/W
		Power down IOUT2 replica when I2_ON is off (other channel 2 settings may affect replica power down timing) 0: no power down 1: powered down	Volatage at REGREF1 when replica is powered down 0: 0 V 1: AHVDD	REGREF1 outputstate. This bit will only take affect if 0x0Ah[0]=1 **1:** REGREF2 is high impedance **0:** 0x0Ah[6] determines state	1: Reduces tail current (gain is reduced to 0.6x) 0: Normal operation	00: 70 01: 32 10: 15 11: 7		Select gm call polarity 1: normal 0: swapped	power down REGREF1 1: power down 0: normal operation		
0Bh	regref0_ctrl	enpd_rep0	rep_pd_pol	hi_z	gm_tail	gain[1:0]		pol_swap	pd_regref0	00000000	R/W
		Power down IOUT2 replica when I2_ON is off (other channel 2 settings may affect replica power down timing) 0: no power down 1: powered down	Volatage at REGREF0 when replica is powered down 0: 0 V 1: AHVDD	REGREF0 outputstate. This bit will only take affect if 0x0Bh[0]=1 **1:** REGREF2 is high impedance **0:** 0x0Bh[6] determines state	1: Reduces tail current (gain is reduced to 0.6x) 0: Normal operation	00: 70 01: 32 10: 15 11: 7		Select gm call polarity 1: normal 0: swapped	power down REGREF0 1: power down 0: normal operation		
0Ch	tempsens_ctrl	Reserved	pd_temp	Temp_Sensor_Offset				Temp_Sensor_Gain		00000000	R/W
			0: Normal Operation 1: Power down temp sensor	Calibrate Temp Sensor Offset 0000: Default 0001: +1 count 0001: +2 counts .... 0111: +7 counts 1111: -1 count 1110: -2 counts ...... 1000: -7 counts				Calibrate Temp Sensor Gain 0X: Default 10: +2.8% 11: -3.2%			
0Dh	tia_ctrl	cpd_comp	Reserved					Rf_ctrl		10101010	R/W
		Additional Cpd compensation for APC 1: 16 pF 0: 0 pF						Controls value of Rf: APC TIA gain control: 11: 20kOhms 10/01: 40kOhms 00: 60kOhms			

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
0Eh	apc_fe_ctrl	Reserved	highcur_en		Reserved				pd_TIA	00001010	R/W
			For common anode 00 -> 0.75 mA 01 -> 1.0 mA 10 ->1.25 mA 11-> 1.5 mA For common cathode x0-> 125 µA x1-> 187 µA						1: power down TIA (Open Loop Mode) 0: TIA active (Closed Loop Mode)		
0Fh	reserved									00000000	R/W
10h	reserved									00000000	R/W
11h	iout2_msb	iout2_gain[11:8]				iout2_offset[11:8]				00000000	R/W
		IOUT2 gain MSB				IOUT2 offset MSB					
12h	iout2_gain_lsb	iout2_gain[7:0]								00000000	R/W
		IOUT2 gain LSB									
13h	iout2_offset_lsb	iout2_offset[7:0]								00000000	R/W
		IOUT2 offset LSB									
14h	iout1_msb	iout1_gain[11:8]				iout1_offset[11:8]				00000000	R/W
		IOUT1 gain MSB				IOUT1 offset MSB					
15h	iout1_gain_lsb	iout1_gain[7:0]								00000000	R/W
		IOUT1 gain LSB									
16h	iout1_offset_lsb	iout1_offset[7:0]								00000000	R/W
		IOUT1 offset LSB									
17h	iout0_msb	iout0_gain[11:8]				iout0_offset[11:8]				00000000	R/W
		IOUT0 gain MSB				IOUT0 offset MSB					
18h	iout0_gain_lsb	iout0_gain[7:0]								00000000	R/W
		IOUT0 gain LSB									
19h	iout0_offset_lsb	iout0_offset[7:0]								00000000	R/W
		IOUT0 offset LSB									
1Ah	despeckle_ctrl	despeckle2		despeckle1		despeckle0		Reserved		00000000	R/W
		Controls despeckle on IOUT2: 00: off 01: On with 0 as OFF current 10: On with offset current as the OFF current 11: On with (offset2-offset2_des) as OFF current		Controls despeckle on IOUT1: 00: off 01: On with 0 as OFF current 10: On with offset current as the OFF current 11: On with (offset1-offset1_des) as OFF current		Controls despeckle on IOUT0: 00: off 01: On with 0 as OFF current 10: On with offset current as the OFF current 11: On with (offset0-offset0_des) as OFF current					

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
1Bh	despeckle2	despeckle_on2[3:0]				despeckle_off2[3:0]				00000000	R/W
(see register 0x02h[2:0])		Despeckle on time for for IOUT2 0000=1 320 MHz clock cycle 0001=2 320 MHz clock cycles … 1111=16 320 MHz clock cycles				Despeckle off time for for IOUT2 0000=1 320 MHz clock cycle 0001=2 320 MHz clock cycles … 1111=16 320 MHz clock cycles					
1Ch	despeckle1	despeckle_on1[3:0]				despeckle_off1[3:0]				00000000	R/W
(see register 0x02h[2:0])		Despeckle on time for for IOUT1 0000=1 320 MHz clock cycle 0001=2 320 MHz clock cycles … 1111=16 320 MHz clock cycles				Despeckle off time for for IOUT1 0000=1 320 MHz clock cycle 0001=2 320 MHz clock cycles … 1111=16 320 MHz clock cycles					
1Dh	despeckle0	despeckle_on0[3:0]				despeckle_off0[3:0]				00000000	R/W
(see register 0x02h[2:0])		Despeckle on time for for IOUT0 0000=1 320 MHz clock cycle 0001=2 320 MHz clock cycles … 1111=16 320 MHz clock cycles				Despeckle off time for for IOUT0 0000=1 320 MHz clock cycle 0001=2 320 MHz clock cycles … 1111=16 320 MHz clock cycles					
1Eh	offset0_des_msb	Reserved				iout2_off_desp[11:8]				00000000	R/W
						IOUT2 offset current negative offset for despeckle (MSB)					
1Fh	offset2_des_lsb	iout2_off_desp[7:0]								00000000	R/W
		IOUT2 offset current negative offset for despeckle									
20h	offset1_des_msb	Reserved				iout1_off_desp[11:8]				00000000	R/W
						IOUT1 offset current negative offset for despeckle (MSB)					
21h	offset1_des_lsb	iout1_off_desp[7:0]								00000000	R/W
		IOUT1 offset current negative offset for despeckle									
22h	offset0_des_msb	Reserved				iout0_off_desp[11:8]				00000000	R/W
						IOUT0 offset current negative offset for despeckle (MSB)					
23h	offset0_des_lsb	iout0_off_desp[7:0]								00000000	R/W
		IOUT0 offset current negative offset for despeckle									
24h	alarm_th2	alarm_th2[7:0]								11111111	R/W
		Alarm threshold for IOUT2 (output DAC MSB)									
25h	alarm_th1	alarm_th1[7:0]								11111111	R/W
		Alarm threshold for IOUT1 (output DAC MSB)									
26h	alarm_th0	alarm_th0[7:0]								11111111	R/W
		Alarm threshold for IOUT0 (output DAC MSB)									

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
27h	reserved	Reserved								00000000	R/W
28h	despeckle_clk	Reserved						despeckle_clk		00000000	R/W
								When 0x02[2:0]=100b: 00 => 320 MHz (Laser mode =>despeckle) 01 => 94 MHz 10 => 160 MHz 11 => 43 MHz (LED mode => power saving)			
						APC REGISTERS					
29h	loop_ctrl	iturnon2	iturnon1	iturnon0	Reserved	loop_clk	apc2_freeze	apc1_freeze	apc0_freeze	00000000	R/W
		Initial IOUT2 DAC is set to: 1: 0 0: offset+gain current	Initial IOUT1 DAC is set to: 1: 0 0: offset+gain current	Initial IOUT0 DAC is set to: 1: 0 0: offset+gain current		PWM and MPG clock 1: Use external clock input (CLK_IN) 0: use internal oscillator	1: freeze APC (both gain and offset) for IOUT2 0: normal operation	1: freeze APC (both gain and offset) for IOUT1 0: normal operation	1: freeze APC (both gain and offset) for IOUT0 0: normal operation		
2Ah	target2_msb	Reserved			target2[12:8]					00000000	R/W
					MSB target DAC for gain of IOUT2						
2Bh	target2_lsb	target2[7:0]								00000000	R/W
		LSB target DAC for gain of IOUT2									
2Ch	target2ith_msb	Reserved			target2_ith[12:8]					00000000	R/W
					MSB target DAC for offset of IOUT2						
2Dh	target2ith_lsb	target2_ith[7:0]								00000000	R/W
		LSB target DAC for offset of IOUT2									
2Eh	target1_msb	Reserved			target1[12:8]					00000000	R/W
					MSB target DAC for gain of IOUT1						
2Fh	target1_lsb	target1[7:0]								00000000	R/W
		LSB target DAC for gain of IOUT1									
30h	target1ith_msb	Reserved			target1_ith[12:8]					00000000	R/W
					MSB target DAC for offset of IOUT1						
31h	target1ith_lsb	target1_ith[7:0]								00000000	R/W
		LSB target DAC for offset of IOUT1									
32h	target0_msb	Reserved			target0[12:8]					00000000	R/W
					MSB target DAC for gain of IOUT0						
33h	target0_lsb	target0[7:0]								00000000	R/W
		LSB target DAC for gain of IOUT0									

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
34h	target0ith_msb	Reserved			target0_ith[12:8]					00000000	R/W
					MSB target DAC for offset of IOUT0						
35h	target0ith_lsb	target0_ith[7:0]								00000000	R/W
		LSB target DAC for offset of IOUT0									
36h	apc2_ctrl2	Tck_init2[1:0]		Tck_mid2[1:0]		Tck_min2[1:0]		Tck_div2[1:0]		00000000	R/W
		Initial clock count for IOUT2 00: 0 01: 63 10: 127 11: 255		Mid clock count for IOUT2 00: 0 01: 31 10: 63 11: 127		Clock counts for IOUT2 at min step 00: 0 01: 31 10: 63 11: 127		Clock counts to enable clock divider for IOUT2 00: 0 01: 63 10: 127 11: 255			
37h	apc2_ctrl1	Step_init2[1:0]		Step_mid2[1:0]		RSVD		ck_div2[1:0]		00000000	R/W
		Initial step size in LSB of IOUT2 00: 1 01: 8 10: 16 11: 32		Mid step size in LSB of IOUT2 00: 1/2 of Step_init 01: 1/4 of Step_init 10: reserved 11: reserved				Clock divider for IOUT2 00: 1 01: 4 10: 8 11: 16			
38h	apc2_ctrl0	Dec2[2:0]			apc_offset	line_mode2	apc2_ch		RSVD	00000000	R/W
		Digital filter decimation factor for IOUT2: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128			1: update IOUT2 offset during blanking following I2_ON 0: do not update and output 0 current during blanking	Line mode for IOUT2 1: OUT2 on only during CLK_IN=H 0: Ignore CLK_IN	Selects APC input for IOUT2 00: APC_IN0 01: APC_IN1 10: APC_IN2 11: disable APC				
39h	reserved	Reserved								00000000	R/W
3Ah	apc1_ctrl2	Tck_init1[1:0]		Tck_mid1[1:0]		Tck_min1[1:0]		Tck_div1[1:0]		00000000	R/W
		Initial clock count for IOUT1 00: 0 01: 63 10: 127 11: 255		Mid clock count for IOUT1 00: 0 01: 31 10: 63 11: 127		Clock counts for IOUT1 at min step 00: 0 01: 31 10: 63 11: 127		Clock counts to enable clock divider for IOUT1 00: 0 01: 63 10: 127 11: 255			
3Bh	apc1_ctrl1	Step_init1[1:0]		Step_mid1[1:0]		Reserved		ck_div1[1:0]		00000000	R/W
		Initial step size in LSB of IOUT1 00: 1 01: 8 10: 16 11: 32		Mid step size in LSB of IOUT1 00: 1/2 of Step_init 01: 1/4 of Step_init 10: reserved 11: reserved				Clock divider for IOUT1 00: 1 01: 4 10: 8 11: 16			

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
3Ch	apc1_ctrl0	Dec1[2:0]			apc_offset	line_mode1	apc1_ch		Reserved	00000000	R/W
		Digital filter decimation factor for IOUT1: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128			1: update IOUT1 offset during blanking following I1_ON 0: do not update and output 0 current during blanking	Line mode for IOUT1 1: OUT1 on only during CLK_IN=H 0: Ignore CLK_IN	Selects APC input for IOUT1 00: APC_IN0 01: APC_IN1 10: APC_IN2 11: disable APC				
3Dh	reserved	Reserved								00000000	R/W
3Eh	apc0_ctrl2	Tck_init0[1:0]		Tck_mid0[1:0]		Tck_min0[1:0]		Tck_div0[1:0]		00000000	R/W
		Initial clock count for IOUT0 00: 0 01: 63 10: 127 11: 255		Mid clock count for IOUT0 00: 0 01: 31 10: 63 11: 127		Clock counts for IOUT0 at min step 00: 0 01: 31 10: 63 11: 127		Clock counts to enable clock divider for IOUT0 00: 0 01: 63 10: 127 11: 255			
3Fh	apc0_ctrl1	Step_init0[1:0]		Step_mid0[1:0]		Reserved		ck_div0[1:0]		00000000	R/W
		Initial step size in LSB of IOUT0 00: 1 01: 8 10: 16 11: 32		Mid step size in LSB of IOUT0 00: 1/2 of Step_init 01: 1/4 of Step_init 10: reserved 11: reserved				Clock divider for IOUT0 00: 1 01: 4 10: 8 11: 16			
40h	apc0_ctrl0	Dec0[2:0]			apc_offset	line_mode0	apc0_ch		Reserved	00000000	R/W
		Digital filter decimation factor for IOUT0: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128			1: update IOUT0 offset during blanking following I0_ON 0: do not update and output 0 current during blanking	Line mode for IOUT0 1: OUT0 on only during CLK_IN=H 0: Ignore CLK_IN	Selects APC input for IOUT0 00: APC_IN0 01: APC_IN1 10: APC_IN2 11: disable APC				
41h	reserved	RSVD								00000000	R/W
42h	dec_off_ctrl	Reserved					DecOff[2:0]			00000001	R/W
							Digital filter decimation factor for offset current: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128				

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
43h	clk_div	clk_div_pwm[3:0]				clk_div_mpg[3:0]				00000000	R/W
		PWM clock divider 0000 = 1 0001 = 2 0010 = 4 0011 = 16 0100 = 256 0101 = 512 0110 = 1024 0111 = 2048				MPG clock divider 0000 = 1 0001 = 2 0010 = 4 0011 = 16 0100 = 256 0101 = 512 0110 = 1024 0111 = 2048					
44h	pwm_msb	Reserved		on_count2[9:8]		on_count1[9:8]		on_count0[9:8]		00000000	R/W
				PWM IOUT2 (msb)		PWM IOUT1 (msb)		PWM IOUT0 (msb)			
45h	pwm2	on_count2[7:0]								00000000	R/W
		PWM on count lsb for IOUT2									
46h	pwm1	on_count1[7:0]								00000000	R/W
		PWM on count lsb for IOUT1									
47h	pwm0	on_count0[7:0]								00000000	R/W
		PWM on count lsb for IOUT0									
48h	mpg_off_msb	Reserved		pulse_off2[9:8]		pulse_off1[9:8]		pulse_off0[9:8]		00000000	R/W
				MPG off IOUT2 (msb)		MPG off IOUT1 (msb)		MPG off IOUT0 (msb)			
49h	mpg_off2	pulse_off2[7:0]								00000000	R/W
		MPG pulse off lsb for IOUT2									
4Ah	mpg_off1	pulse_off1[7:0]								00000000	R/W
		MPG pulse off lsb for IOUT1									
4Bh	mpg_off0	pulse_off0[7:0]								00000000	R/W
		MPG pulse off lsb for IOUT0									
4Ch	mpg_on_msb	Reserved		pulse_on2[9:8]		pulse_on1[9:8]		pulse_on0[9:8]		00000000	R/W
				MPG on IOUT2 (msb)		MPG on IOUT1 (msb)		MPG on IOUT0 (msb)			
4Dh	mpg_on2	pulse_on2[7:0]								00000000	R/W
		MPG pulse on lsb for IOUT2									
4Eh	mpg_on1	pulse_on1[7:0]								00000000	R/W
		MPG pulse on lsb for IOUT1									
4Fh	mpg_on0	pulse_on0[7:0]								00000000	R/W
		MPG pulse on lsb for IOUT0									
5Dh	checksum	Checksum								01010101	R/W
		Checksum									
5Fh	DL_done	Reserved				dl_done				00000101	R/W
						1010b: download done anything else: download not done					

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
REGISTERS only accessible to an external uC											
80h	soft_reset	Soft reset								00000000	R
		Writing AA causes a reset (this register will clear after reset) All registers returned to default value									
81h	checksum_cal	Checksum calculated									
		Checksum of 96 bytes calculated by M08886 for debugging purposes									
82h	chip_id	Revision identification:				Chip identification				00000000	R
		0001 for -13 die				0110					
83h	temp	temp[7:0]								00000000	R
		Temperature readback									
84h	rb_iout2_msb	iout2_gain[11:8]				iout2_offset[11:8]				00000000	R
		read back IOUT2 gain MSB				read back IOUT2 offset MSB					
85h	rb_iout2_gain_lsb	iout2_gain[7:0]								00000000	R
		read back IOUT2 gain LSB									
86h	rb_iout2_offset_lsb	iout2_offset[7:0]								00000000	R
		read back IOUT2 offset LSB									
87h	rb_iout1_msb	iout1_gain[11:8]				iout1_offset[11:8]				00000000	R
		read back IOUT1 gain MSB				read back IOUT1 offset MSB					
88h	rb_iout1_gain_lsb	iout1_gain[7:0]								00000000	R
		read back IOUT1 gain LSB									
89h	rb_iout1_offset_lsb	iout1_offset[7:0]								00000000	R
		read back IOUT1 offset LSB									
8Ah	rb_iout0_msb	iout0_gain[11:8]				iout0_offset[11:8]				00000000	R
		read back IOUT0 gain MSB				read back IOUT0 offset MSB					
8Bh	rb_iout0_gain_lsb	iout0_gain[7:0]								00000000	R
		read back IOUT0 gain LSB									
8Ch	rb_iout0_offset_lsb	iout0_offset[7:0]								00000000	R
		read back IOUT0 offset LSB									
8Dh	alarm_ctrl	alarm2	alarm1	alarm0	Reserved					00000000	R/W
		Alarm for IOUT2	Alarm for IOUT1	Alarm for IOUT0							
8Eh	reserved	Reserved								00000000	R/W

Table 3-1. M08886 Registers

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
90h	strbalrm_ctrl	Reserved			reg_spl_dis	Reserved		strb_iout	clear_alarm	00000000	R/W
					Disables register sampling: 1: Disable register sampling (cannot read/ write to any register except 90h) 0: Normal operation (all registers are accessible)			1: strobes iout current before read0back 0: Normal	1: Clear alarm 0: Normal		
91h	Reserved	Reserved								00000000	R/W

M/A-COM Technology Solutions Inc. All rights reserved.

Information in this document is provided in connection with M/A-COM Technology Solutions Inc ("MACOM") products. These materials are provided by MACOM as a service to its customers and may be used for informational purposes only. Except as provided in MACOM's Terms and Conditions of Sale for such products or in any separate agreement related to this document, MACOM assumes no liability whatsoever. MACOM assumes no responsibility for errors or omissions in these materials. MACOM may make changes to specifications and product descriptions at any time, without notice. MACOM makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF MACOM PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. MACOM FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. MACOM SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

MACOM products are not intended for use in medical, lifesaving or life sustaining applications. MACOM customers using or selling MACOM products for use in such applications do so at their own risk and agree to fully indemnify MACOM for any damages resulting from such improper use or sale.