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Synchronizing Multiple ADCs Using JESD204B

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Abstract

Many communications, instrumentation, and signal acquisition systems require the ability to simultaneously sample analog input signals across multiple analog-to-digital converters (ADCs). The sampled data then needs to be processed with the expectation of synchronization across these inputs that each have their own various different latencies. This has historically been a difficult challenge for system designers to meet with low voltage digital signaling (LVDS) and parallel output ADCs.

JESD204B provides a framework for high speed serial data to be sent along one or more differential signal pairs, such as an output of an ADC. There is an inherent scheme in the interface to achieve coarse alignment across lanes within the JESD204B specification. Data is partitioned into frames with boundaries that are continuously sent to the receiver. The JESD204B Subclass 1 interface has provisions for data alignment down to the sample level across multiple serial lane links or multiple ADCs by using a system reference event signal (SYSREF) to synchronize internal framing clocks in both the transmitter and receiver. This creates a deterministic latency for the devices using the JESD204B link. However, there are still many challenges that a system designer must overcome to achieve full timing closure for sampling synchronization, such as PCB layout considerations, matched clock, and SYSREF generation to meet timing, SYSREF periodicity, and digital FIFO delays.

The designer must decide how the device clock and SYSREF signal will be created and distributed throughout the system. Ideally, the device clock and SYSREF should be of the same swing level and offset to prevent inherent skew at the component input pin. The update rate of the SYSREF event will need to be determined as either a single event at startup or a recurring signal that may occur at any time synchronization is needed. Taking the maximum clock and SYSREF signal skew into consideration, careful PCB layout is needed to meet setup and hold timing across boards, connectors, backplanes, and various components. Finally, digital FIFO design and signals traversing across multiple clock domains create inherent digital buffer skew within JESD204B transmitters and receivers that must be accounted for and removed in back-end data processing.

System clock generation can come from several sources such as crystals, VCOs, and clock generation or clock distribution chips. While the particular system performance will dictate the clocking needs, one must use multiple synchronous ADCs to produce a SYSREF signal that is source synchronous to the input clock. This makes the clock source selection an important consideration in order to be able to latch this system reference event with a known clock edge at a particular point in time. If the SYSREF signal and clock are not phased locked, this cannot be achieved.

An FPGA can be used to provide a SYSREF event to the system. However, unless it also uses and synchronizes to the master sample clock that is sent to the ADCs, it will be difficult to phase align the SYSREF signal from the FPGA to the clock. An alternate approach is to provide the SYSREF signal from a clock generation or clock distribution chip that can phase align this signal to multiple clocks that are sent throughout the system. Using this method, the SYSREF event can be a one-shot event at startup or a recurring signal depending upon the system requirements.

As long as deterministic latency remains constant within the system across ADCs and FPGAs, additional SYSREF pulses may not be needed except to help frame particular system data. Hence, a periodic SYSREF pulse for clock alignment can be ignored or filtered until the time at which synchronization is lost. A marker sample for the occurrence of SYSREF could alternately be maintained without resetting the JESD204B link.

In order to initiate a known deterministic starting point for the ADC channels, the system engineer must be able to close timing for the SYSREF event signal distributed across the system. This means that the expected setup and hold time, relative to the clock, must be met without violation. Use of a relatively long SYSREF pulse that spans multiple clock cycles can be used to meet the hold time requirement, so long as the setup time to the first required clock can also be met. Careful attention to PCB layout is critical in this effort to maintain matched trace lengths for clocks and SYSREF within the system for minimum skew. This may be the most difficult part of achieving synchronous sampling processing across channels. The effort will only get progressively more challenging as ADC encode clock rates increase and multiboard systems become more complex.

SYSREF to clock board skew at components across boards and connectors must be deterministically known for each device by the system engineer. Any remaining interdevice digital and clock skew delays need to be effectively nulled in the FPGA or ASIC. Back-end processing can change the sample order across ADCs and introduce any needed realignment to prepare the data for further synchronized processing. Correction for interdevice sample skew can be accomplished by delaying the fastest data samples and transmitter latency to align with the slowest data samples in the back-end FPGA or ASIC. For complex systems, this may involve multiple FPGAs or ASICs where each needs to communicate their total interdevice sample latency for final alignment. By introducing appropriate elastic buffer delays in the JESD204B receiver(s) to accommodate each specific transmitter latency delay, the interdevice sample skews can be aligned with known determinism across a system.

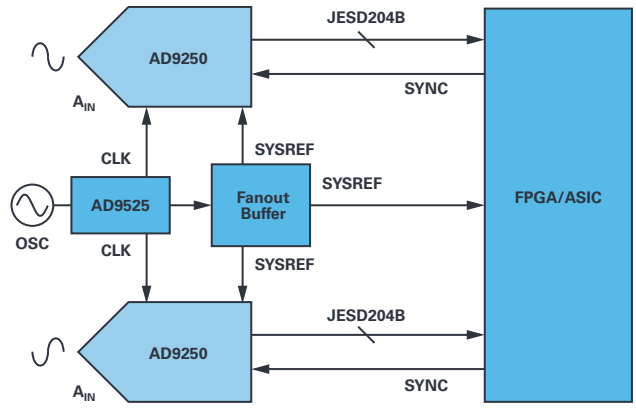

Figure 1. Diagram showing the AD9250, the AD9525, and an FPGA.

The AD9250 is a 250 MSPS 14-bit dual ADC from Analog Devices that supports the JESD204B interface in a Subclass 1 implementation. This subclass allows analog sample synchronization across ADCs using the SYSREF event signal. The AD9525 is a low jitter clock generator that not only provides seven clock outputs up to 3.1 GHz but is also able to synchronize a SYSREF output signal based on user configurations. These two products, coupled with a selection of fanout buffer products from Analog Devices, provide the framework to accurately synchronize and align multiple ADC data sent to an FPGA or ASIC for processing.

About the Author

Ian Beavers is a product engineering manager for the Automation Energy and Sensors Team located at Analog Devices, Greensboro, NC. He has worked for the company since 1999. Ian has over 20 years of experience in the semiconductor industry. Ian earned a bachelor's degree in electrical engineering from North Carolina State University and an M.B.A. from the University of North Carolina at Greensboro. He can be reached at *ian.beavers@analog.com*.

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