Product Update

Errata for Z8 Encore! XP® F6482 Series Devices

F6482 Series MCU for All Date Codes

The errata listed in Table 3 are found in all F6482 Series devices regardless of package date code. When reviewing the following errata, Zilog recommends that you download the most recent version of the Z8 Encore! XP F6482 Series Product Specification (PS0294) from the Zilog website.

Table 1. Errata to F6482 Series Devices

No.	Summary	Detailed Description
1	Information page erase attempt affects main memory	A user code attempt to erase the locked Zilog Flash information page results in erase of main memory Page 0. **Suggested Workarounds:** 1. Ensure INFO_EN=0 in the Flash Page Select Register prior to erasing a Flash page. 2. Block protect main memory Page 0. To block protect Page 0, in the Flash Block Protection Register configure FBP_EN=1 and FBPS=01h. FBPS identifies the page number of the first page that is not protected. All pages below this page are protected.
2	MOSI0 (PA4) and SCK0 (PA5) are open drain only	MOSI0 on PA4 and SCK0 on PA5 are open drain for an SPI0 master, regardless of the WOR setting in the ESPI0 Control Register. In addition, for SCK0 on PA5 to function properly for a SPI0 slave, it is necessary to set CLKPOL=1 in the ESPI0 Control Register. **Suggested Workarounds:** 1. Use internal or external pull-ups. 2. Use PC4 and PC5 as MISO0 and SCK0 instead of PA4 and PA5. 3. If available, use SPI1 instead of SPI0.
3	External reset can occur upon Stop Mode Recovery	Upon Stop Mode Recovery, the Z8F6482 drives then releases the PD0/$\overline{\text{RESET}}$ pin if the pin is configured as $\overline{\text{RESET}}$, If this pin does not return to a high level within 2 System Clocks after it is released, an external reset can be detected resulting in a System Reset. **Suggested Workarounds:** 1. If an external reset function is not needed, configure the PD0/$\overline{\text{RESET}}$ pin to be PD0 via the Port D GPIO Alternate Function registers. 2. Use a low value external pull-up resistor on the PD0/$\overline{\text{RESET}}$ pin. such that the RC time constant is less than two System Clock periods. 3. Prior to entering Stop Mode, configure System Clock to be a low frequency such as 1MHz. For example, by increasing the System Clock divider (CLKCTL Register) or by loading a previously stored low frequency DCO control word and select the DCO as System Clock. After Stop Mode Recovery, select the desired System Clock source and frequency.

Table 1. Errata to F6482 Series Devices (Continued)

No.	Summary	Detailed Description
4	ADC and DAC linearity may degrade at low levels of internal AVDD as VREF+	ADC and DAC INL/DNL performance may degrade somewhat for REFSEL=00 (VREF+ internal connection to AVDD) when AVDD < 2.25V **Suggested Workarounds:** 1. Maintain AVDD ≥ 2.25V. 2. Select an alternate VREF+ such as an external reference on the VREF+ pin or an internal voltage reference. Note that AVDD can be connected to the VREF+ pin and used as an external VREF+.
5	Temperature Sensor Output Error can exceed specification	Temperature Sensor Output Error can exceed specification. **Suggested Workaround:** Do not use in applications that require a high degree of temperature sensor accuracy.
6	Less than ideal FLL frequency locking robustness	Instantaneous FLL frequency error can be greater than expected based on the DCO resolution and the average FLL frequency can exhibit error. Furthermore, maximum FLL lock time, while not specified can exceed the typical specification dramatically. **Suggested Workaround:** 1. If a high accuracy System CLock frequency and or faster lock time is needed, use an external HFXO with or without the PLL as System Clock.
7	Delay is needed prior to re-enabling TImer in any One-Shot Mode if Pclk or the WTO is Timer clock	After reaching the reload value and generating an interrupt, the Timer requires one Timer Clock for processing prior to being re-enabled. If the selected Timer Clock is Pclk or the WTO, it is possible for software to attempt to re-enable the Timer during this processing time. If this occurs, the re-enable attempt is ignored. **Suggested Workaround:** 1. Add one Timer Clock of delay to the interrupt service routine before setting TEN=1.
8	ADC outside window IRQ always asserts for 12-bit resolution conversions	12-bit resolution conversions generate an outside window interrupt even the ADC result is within the Threshold Window. ADCCTL0[4] = 0 generates interrupt if the ADC data is outside Threshold Window. **Suggested Workaround:** 1. Select 14-bit conversions and enable averaging by setting RESOLUT=1 and AVE=1.
9	Averaging must be selected for 14-bit resolution ADC window checking	ADC window check will behave erroneously for 14-bit resolution conversions if averaging is disabled. **Suggested Workaround:** 1. Enable averaging by setting AVE=1.
10	ADC scan sequence performs an extra conversion when the ANA0 is selected	ADC scans starting with selected channel 0 will repeat the channel 0 conversion before continuing the scan sequence. This occurs only once at the start of the scanning sequence and only if ANA0 is one of the channels selected. **Suggested Workaround:** 1. When SCAN=1 and ADCINSL[0]=1 then discard first ADC conversion after starting the ADC.

Table 1. Errata to F6482 Series Devices (Continued)

No.	Summary	Detailed Description

11	Brief increase in IDDS1 and IDDS2 after entering Stop Mode	Shortly after entering Stop Mode, IDDS1 and IDDS2 can temporarily increase and exceed specification by several hundred microamperes. This excess Stop Mode IDD typically subsides within 30ms of entering Stop Mode.
		Suggested Workaround:
		1. IConfigure the contents of the 3 address bytes following the STOP instruction to %00.
		When the MCU exits Stop mode, it begins code execution at the address defined by the Reset vector.
		Example:
		`STOP ; Enter Stop mode`
		`DW %00, %00, %00 ; Define the 3 addresses following the Stop instruction as %00`

F6482 Series MCU for Date Codes 2118 and later

The errata listed in Table 3 are found in the F6482 Series devices with date codes prior to and including date code 2118. When reviewing the following errata, Zilog recommends that you download the most recent version of the Z8 Encore! XP F6482 Series Product Specification (PS0294) from the Zilog website.

NOTE: This section also applies to some devices with Date Codes 2119 through 2122. Please see PCN ZAC21-0051 for details.

Table 2. Errata to F6482 Series Devices

No.	Summary	Detailed Description
1	SPI0 slave always drives MISO0 on PC1	If SPI0 is enabled as a slave for PC1/ANA5/C0INN/MISO0 and SPI0 is configured for I2S Mode of operation, the only alternate function available is MISO0. **Suggested Workarounds:** 1. If available, use SPI1 instead of SPI0 when PC1/ANA5/C0INN/MISO0 is required for another function. 2. Use Comparator 1 if an external comparator negative input is required.
2	ANA3 not available when SPI0 Master is enabled	ANA3 is not available when SPI0 is enabled as a master. In this case, PC2/ANA3/SS0– can be used as PC2 or SS0–. It is common to use SS0– as an output when SPI0 is a master. **Suggested Workaround:** If available, use SPI1 instead of SPI0.
3	WDT Reset occasionally missed or causes device hang	If the WDT is configured to generate a System Reset (WDT_RES=1), upon WDT time-out, occasionally the time-out can be missed or the device can hang. Another reset source such as external reset or POR is required to clear the hang. **Suggested Workarounds:** 1. Configure the WDT to generate an interrupt (WDT_RES=0). In the WDT interrupt service routine, reconfigure all control registers back to their default values then jump to the reset vector. 2. Connect externally an unused GPIO to the Reset pin and drive the GPIO low in the WDT interrupt service routine.
4	RTC alarms occasionally missed	Due to synchronization error, RTC alarms are occasionally missed. **Suggested Workaround:** 1. Wait for the next alarm. 2. Poll the RTC to read the current counter register values and compare them against the programmed alarm register values. If the current count is greater than the alarm value, an alarm has been missed and software can generate the interrupt by setting the IRQ1[0] Register bit.
5	Failure to power up	At POR, VBG can be connected to a GPIO (PB2) and loaded externally, preventing Vcore power up **Suggested Workaround:** 1. Float PB2 during power-up.

Table 2. Errata to F6482 Series Devices (Continued)

No.	Summary	Detailed Description
6	PD1 Data out forced to Zero	The PD1 Data out is forced to Zero when PD2 alternate function is selected in the PDAFS1 Register. **Suggested Workarounds:** 1. If the PD1 alternate function is being used, select a GPIO other than PD1 for outputting data. 2. Use an analog input other than PD2.
7	FLL enabled at Reset	Upon Reset, the FLLEN bit in the CLKCTL5 Register is set, enabling the FLL. **Suggested Workaround:** 1. If running the FLL is not desired, clear the FLLEN bit in the CLKCTL5 Register.

F6482 Series MCU for Date Codes 1447 and later

The errata listed in Table 3 are found in the F6482 Series devices with date codes prior to and including date code 1447. When reviewing the following errata, Zilog recommends that you download the most recent version of the Z8 Encore! XP F6482 Series Product Specification (PS0294) from the Zilog website.

Table 3. Errata to F6482 Series Devices

No.	Summary	Detailed Description
1	IPO does not meet tolerance targets	The 2% IPO tolerance target is exceeded. Current tolerance is ~3.5%. **Suggested Workaround:** If a higher accuracy clock is required, use an external clock source instead of the IPO.
2	ADC linearity can exceed specification at higher ADC clock rates	ADC INL and DNL increase with increasing ADC clock frequency at an ADC clock frequency of 1.5MHz. The INL and DNL specifications can be exceeded at an ADC clock frequencies of approximately 2MHz and higher. **Suggested Workaround:** Use an ADC clock frequency of less than 2MHz.
3	ADC linearity can exceed specification when V_{REF} and V_{IN} are close to AV_{DD}	ADC INL and DNL performance degrades at higher ADC input levels (V_{IN}) when using when $V_{REF}+ \geq 15/16 * AV_{DD}$ and the following input modes: 1. Single-Ended Input Mode (INMODE=00). 2. Differential Input Mode (INMODE=01). **Suggested Workarounds:** 1. If using $V_{REF}+ = AV_{DD}$, maintain $V_{IN} < 15/16 * V_{REF}+$. 2. Use $V_{REF}+ < 15/16 * AV_{DD}$. 3. Use the following input modes: Unbalanced differential with translation buffer (INMODE=10) or Single-Ended with translation buffer (INMODE=11).
4	ADC linearity ADC linearity can exceed specification near mid-range in Single-Ended Input Mode	In Single-Ended Input Mode (INMODE=00), the ADC INL and DNL performance can exceed specification for codes near the mid-range, specifically from 800H to 930H (12-bit resolution), unless $AV_{DD} \geq 2.7V$ and $V_{REF}+ \leq AV_{DD}-0.5V$. **Suggested Workarounds:** 1. Use an alternate input mode such as Single-Ended Input Mode with translation buffering (INMODE=11). 2. Operate the device with $AV_{DD} \geq 2.7V$ and $V_{REF}+ \leq AV_{DD}-0.5V$.
5	DAC DNL can exceed specification	DAC DNL can exceed specification of <±1LSB at code 3840 by up to 0.5LSB. **Suggested Workarounds:** 1. Use in applications that can accept <±1.5LSB DNL. 2. Employ an input range such that output codes >3839 (decimal) are not used.

Table 3. Errata to F6482 Series Devices (Continued)

No.	Summary	Detailed Description
6	VBIASEN does not enable VBIAS	Setting VBIASEN=1 in the CMPCTL Register does not enable VBIAS. **Suggested Workarounds:** VBIAS is enabled if any of the following are true: 1. A programmable reference is enabled by setting PREFEN=1 and clearing PREFSRC=0 in CMP0CTL1 or CMP1CTL1 registers. 2. An internal reference voltage is selected for the ADC. 3. An internal reference voltage is selected for the DAC and the DAC is enabled. To output VBIAS on the VBIAS pin, select the corresponding GPIO alternate function and set VBIASEN in the CMPCTL Register.
7	Op Amp A PGA gain error exceeds specification	Op Amp A PGA gain network error exceeds specification. The gain is selected using the GAIN field in the AMPACTL1 Register. The nominal gain at some GAIN settings differs from specification. In addition, the gain network tolerance at some GAIN settings differs from specification. Please refer to the below table for details.

GAIN	Specified Gain	Actual Gain
0000	1.5 ± 0.5%	1.49 ± 1.0%
0001	2 ± 0.5%	2 ± 1.5%
0010	2.5 ± 0.5%	2.45 ± 1.0%
0011	3 ± 0.5%	3.05 ± 1.0%
0100	3.75 ± 0.5%	3.55 ± 1.0%
0101	4 ± 0.5%	4 ± 1.0%
0110	5 ± 0.5%	4.55 ± 1.5%
0111	6 ± 0.5%	4.9 ± 1.5%
1000	7.5 ± 0.5%	5.35 ± 1.5%
1001	8 ± 0.5%	5.8 ± 1.5%
1010	10 ± 0.5%	6.4 ± 2.5%
1011	12 ± 1.0%	7.1 ± 2.5%
1100	15 ± 1.0%	8 ± 2.5%
1101	20 ± 1.0%	16 ± 2.5%
1110	30 ± 1.0%	32 ± 3.5%
1111	60 ± 1.0%	64 ± 6.0%

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