Si4708/09 Programming Guide

1. Introduction

1.1. Scope

This document applies to Si4708/09 and example code version 0.1 and greater. Refer to www.skyworksinc.com for example code.

1.2. Purpose

This document is intended to be used with Skyworks “AN230: Si4700/01/02/03 Programming Guide." The purpose of this programming guide is to describe features that are unique to the Si4708/09:

- Device initialization sequence and busmode selection
- Powerup and powerdown sequences
- Hardware control registers

For topics that are not covered in this document, refer to AN230.

This document references the Si4708/09 data sheet and AN230.

1.3. Terminology

SENB or $\overline{\text{SEN}}$—serial enable pin, active low, used only for 3-wire operation.

SDIO—serial data in/data out pin.

SCLK—serial clock pin.

RSTB or $\overline{\text{RST}}$—reset pin, active low.

Device—refers to the Si4708/09.

1.4. Differences between Si4708/09 and Si4700/01/02/03

The Si4708/09 uses a 2.5x2.5 mm 16-pin QFN package. The Si4702/03 and Si4700/01 use 20-pin and 24-pin packages, respectively. For the purpose of programming, the key difference is that the Si4708/09 does not have GPIO1 and GPIO3 pins, and, as a result, the Si4708/09 does not offer an internal oscillator function and only offers bus mode selection with the SENB pin. This necessitates minor differences in the initialization sequence, busmode selection, powerup and powerdown sequences, and hardware control registers for the Si4708/09. Key differences between the Si4708/09 and the Si4700/01/02/03 are presented in bold text.

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2. Hardware Description

2.1. Power, Initialization Sequence, and Busmode Selection

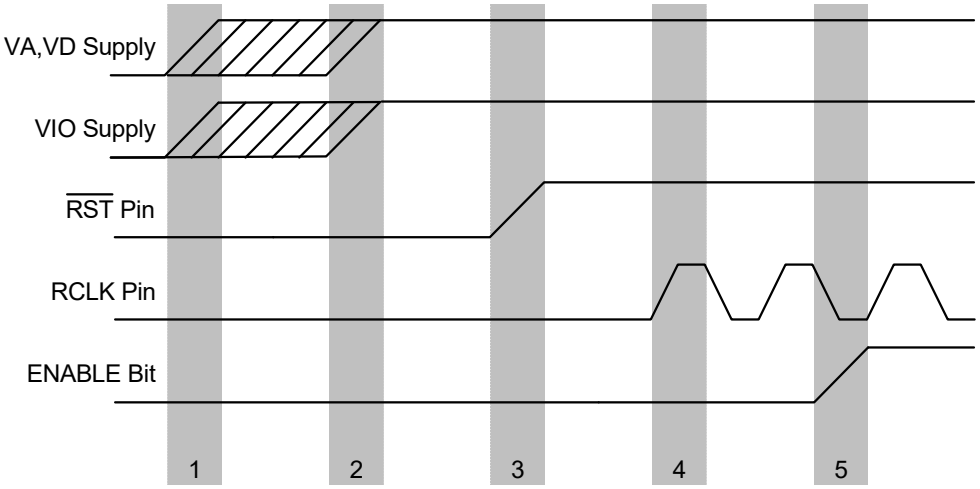


Figure 1. Initialization Sequence

2.1.1. Hardware Initialization

The FM tuner device is capable of communicating using either a 3-wire or 2-wire interface. The selection of this interface is made during the reset sequence.

Figure 1 demonstrates the sequencing of hardware events relative to reset. Figure 2 combines this information with the setting of the ENABLE and DISABLE bits to better describe the possible combinations. The following steps should be used to initialize the device properly.

1. Supply VA and VD.
2. Supply VIO while keeping the RST pin low. Note that power supplies may be sequenced in any order (steps 1 and 2 may be reversed).
3. Configure the SENB pin for bus mode selection. See Figure 3, “Powerup, Powerdown, and Reset Flowchart,” on page 6.
4. Set the RST pin high. The device registers may now be read and written.
5. **Provide RCLK. A delay may be necessary for some external oscillator circuits to ensure that the oscillator has stabilized. Please determine the necessary stabilization time for the clock source in the system.**

Note: The Si4708/09 does not offer an internal oscillator option.

6. Set the ENABLE bit high and the DISABLE bit low to power up the device.

2.1.2. Hardware Powerdown

A powerdown mode is available to reduce power consumption when the part is idle. Setting both the ENABLE bit high and the DISABLE bit high starts the powerdown sequence. This disables analog and digital circuitry while maintaining register configuration and keeping the bus active. Note that the device automatically sets the ENABLE bit low after the internal powerdown sequence completes. Setting the ENABLE bit low directly will cause the device to partially powerdown and should be avoided. See Figure 2. Setting the ENABLE bit high and the DISABLE bit low will bring the device out of powerdown mode and resume normal operation. Refer to Figure 1 for more information.

To power down the device:

1. **Set Register 4 [5:4], [3:2], and [1:0] to 0b10. This step is required for the Si4708/09 to ensure VIO powerdown mode current meets data sheet specifications.**
2. Set the ENABLE bit high and the DISABLE bit high to place the device in powerdown mode. Note that all register states are maintained so long as VIO is supplied and the RST pin is high.

3. Remove VA and VD supplies as needed.

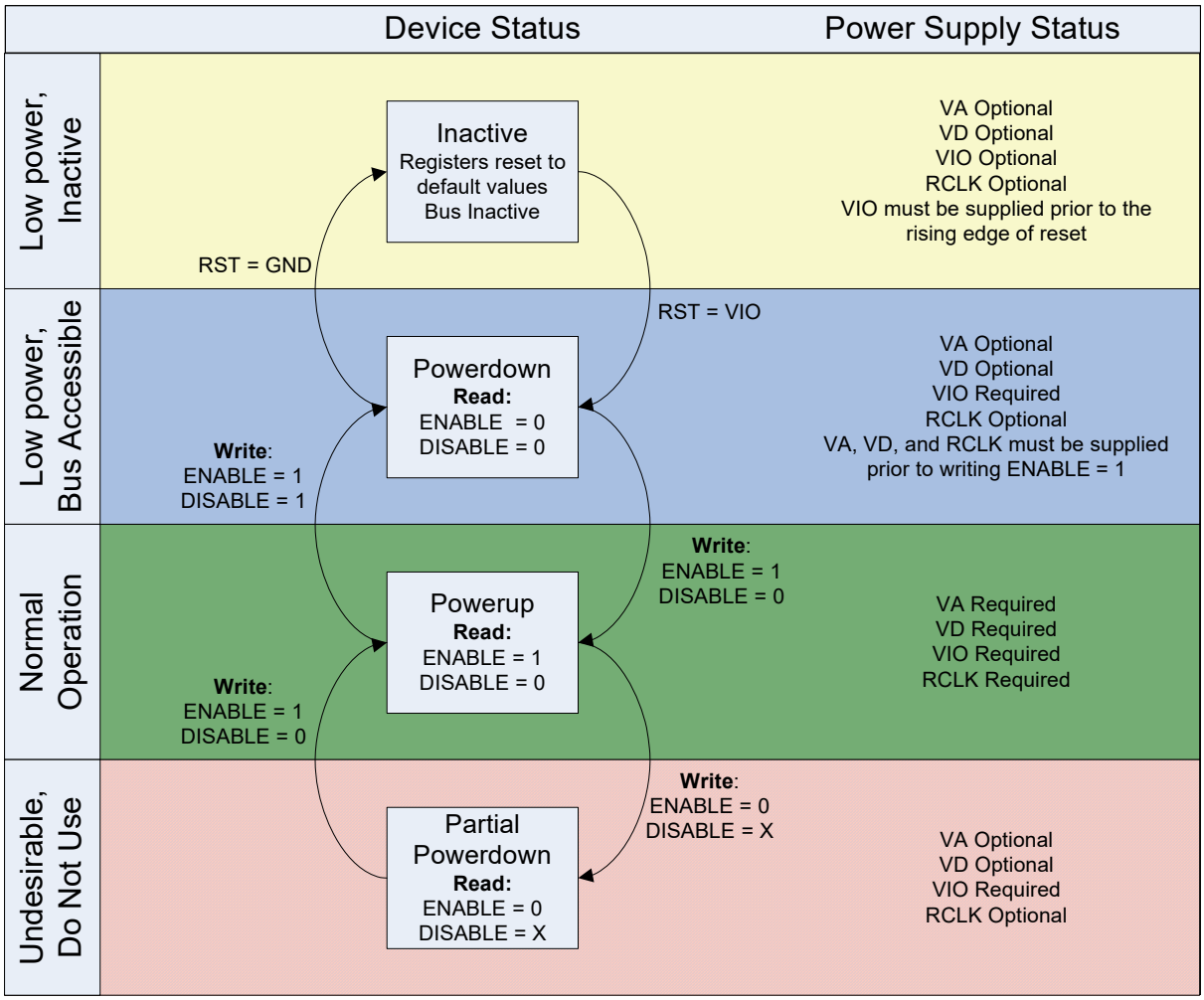
To power up the device (after power down):

Note: VIO is still supplied in this scenario. If VIO is not supplied, refer to 2.1.1. "Hardware Initialization"

1. Supply VA and VD.
2. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

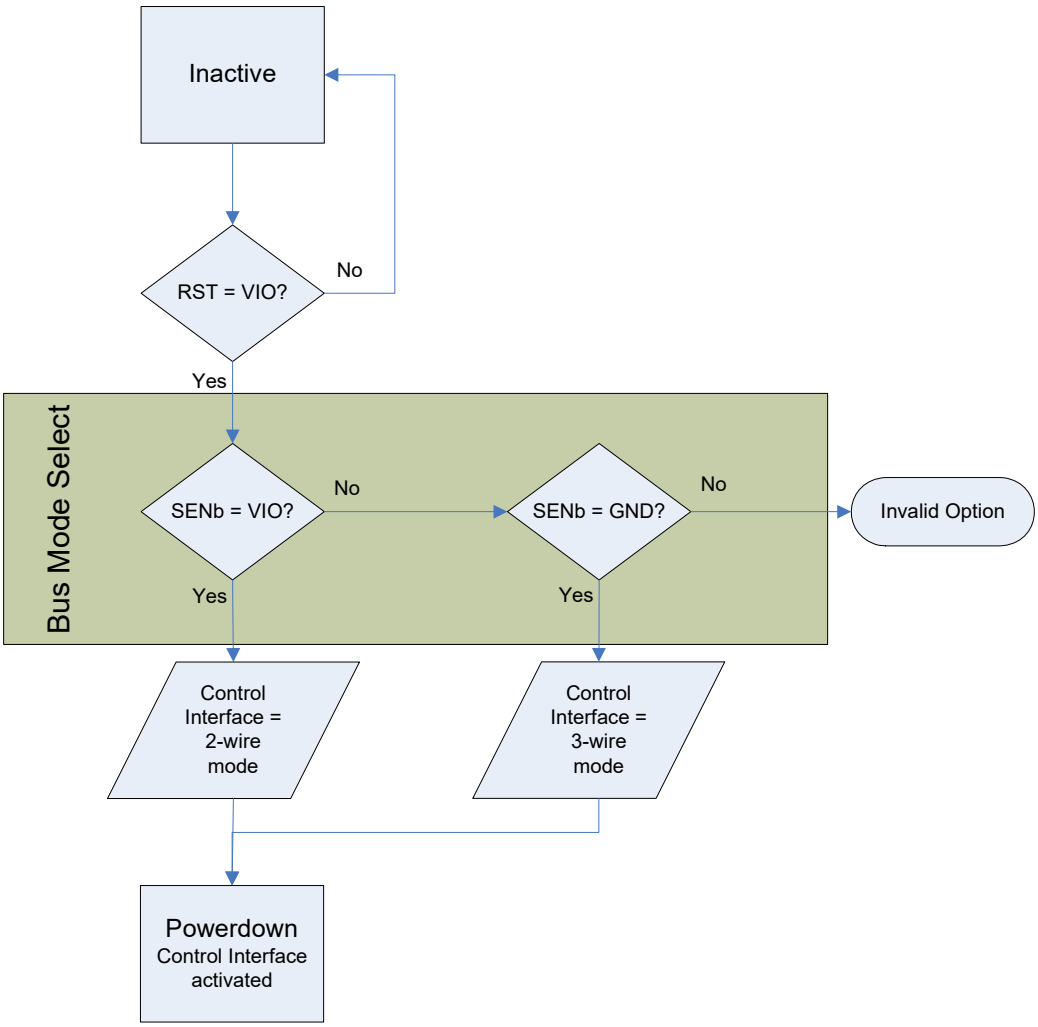
Setting the $\overline{RST}$ pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the $\overline{RST}$ pin high will bring the device out of reset, place the device in powerdown mode, and latch which bus mode will be used to communicate with the device. The bus mode selection is determined by the SENB pin. To select 2-wire operation, the SENB pin must be sampled high by the device on the rising edge of RST. To select 3-wire operation, the SENB pin must be sampled low by the device on the rising edge of RST (See Figure 3). Please refer to the data sheet for more information regarding bus selection and timing requirements of the RST signal.

More details on the register access during powerup and powerdown can be found in Section "3.2.1.ENABLE (02h.0)/DISABLE (02h.6)—Powerup Control" on page 8.



Note: See data sheet for further details.

Figure 2. Powerup, Powerdown, and Reset State Diagram



Note: See data sheet for further details.

Figure 3. Powerup, Powerdown, and Reset Flowchart

2.1.3. Wire Control Interface

For information on the 3-wire control interface, refer to Section 2.2 of “AN230: Si4700/01/02/03 Programming Guide."

2.2. 2-Wire Control Interface

For information on the 2-wire control interface, refer to Section 2.2 of “AN230: Si4700/01/02/03 Programming Guide."

3. Software Configuration

3.1. Registers

The control and status of the device is obtained through bitfields within 16 registers of 16 bits each. The functionality of the bits can be separated into two main categories: control and status. The control bits can be further subdivided into categories of when or how they are used (see Table 1). While the status bits can be classified as static, static after power up, or dynamic after power up (see Table 2). **Note that the Si4708/09 does not offer GPIO1 or GPIO3.**

Table 1. Register Use

Bit(s)	Hardware Control	General Config	Regional Config	End User Adjustable	Seek	Tune
DISABLE	X					
ENABLE	X					
AHIZEN	X					
GPO	X					
RDSIEN	X					
STCIEN	X					
BLNDADJ		X				
DSMUTE		X				
SMUTER		X				
SMUTEA		X				
VOLEXT		X				
SEEKTH		X				
SKSNR		X				
SKCNT		X				
RDSPRF		X				
RDSM		X				
RDS			X			
DE			X			
BAND			X			
SPACE			X			
DMUTE				X		
MONO				X		
VOLUME				X		
SEEKUP					X	
SKMODE					X	
SEEK					X	
TUNE						X
CHAN						X

Table 2. Status Bit Classification

Bit(s)	Static	Static After Power Up	Dynamic After Power Up
PN	X		
MFGID	X		
REV		X	
DEV		X	
FIRMWARE		X	
ST			X
RSSI			X
READCHAN			X
STC			X
SF/BL			X
AFCRL			X
RDSR			X
RDSS			X
BLERA			X
BLERB			X
BLERC			X
BLERD			X
RDSA			X
RDSB			X
RDSC			X
RDSD			X

3.2. Hardware Control Registers

The following set of registers alter the hardware in some way. These registers are typically the first group to be programmed.

3.2.1. ENABLE (02h.0)/DISABLE (02h.6)—Powerup Control

The ENABLE/DISABLE bits are analogous to the on/off buttons of the device. ENABLE=1 turns the device on while DISABLE=1 turns the device off (powerdown mode). When writing the register to place the device into powerdown mode, ENABLE should remain set to 1 while setting DISABLE to 1. The device clears the ENABLE and DISABLE bits, indicating the powerdown mode has been entered.

Table 3 shows the sequence of commands required to powerup the device. Note that address 07h may be written during powerup configuration.

Table 3. Powerup Configuration Sequence

Write address 02h (required). ■ Set the DMUTE bit to disable mute. Optionally mute can be disabled later when audio is needed. ■ Set the ENABLE bit high to set the powerup state. ■ Set the DISABLE bit low to set the powerup state. **Example:** Write data 4001h.
Wait for device powerup (required). ■ Refer to the Powerup Time specification in Table 7 "FM Characteristics" of the data sheet.
Read addresses 00h–01h (optional). ■ **The bits PN[3:0] = 1 indicate the part family: Si4708/09.** ■ The bits MFGID[11:0] = 242h indicate Skyworks as the manufacturer. ■ The bits REV[5:0] = 1 indicates silicon revision B. ■ The bits DEV indicate the identity of the device: DEV = 0010 after powerup = Si4708. DEV = 1010 after powerup = Si4709. ■ The FIRMWARE bits indicate the firmware revision after powerup.
Read addresses 02h-0Fh (optional) ■ Storing the values of each of the 16 registers locally is recommended to simplify manipulation of register bits and to reduce the number of reads/writes to the I/O bus. These are referred to as the shadow registers and can be stored in a 16 word array, `shadow_reg[]`. **Example:** To write bit 15 of register 07h after power up, write 07h as `shadow_reg[0x07] ^ 0x8000`
Write remaining hardware configuration registers (required). **Write the general configuration registers (required).** **Write the regional configuration registers (required).** These registers can be programmed in any order.

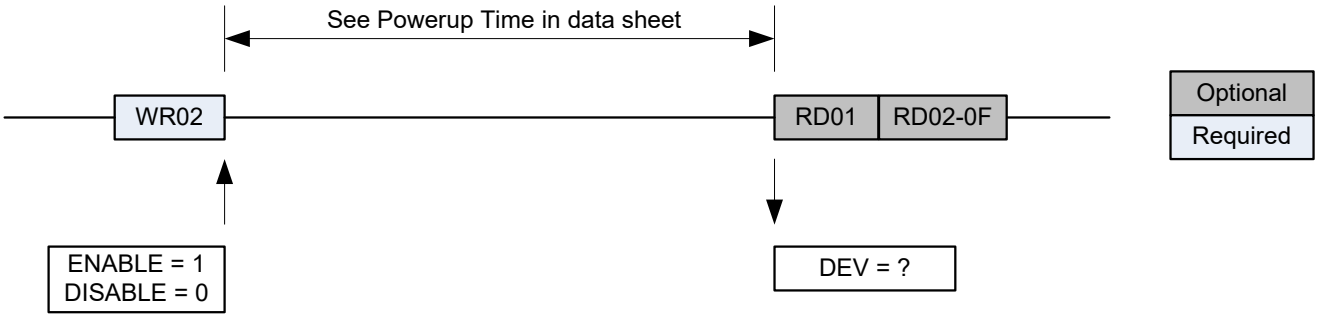


Figure 4. Powerup Timing

Table 4 shows the sequence of commands required to powerdown the device. The tuner can optionally be programmed to place the audio output pins into a high impedance state. If this is desired, set the AHIZEN bit in register 07h prior to setting the disable bit. See AN230, Section "3.2.3.AHIZEN (07h.14)—Audio High-Z Enable" on page 10 for more information. Set Register 4 [5:4] and [1:0] to 10b prior to setting the disable bit.

Table 4. Powerdown Sequence

Write address 07h (optional for LOUT and ROUT Hi-Z). ■ Set AHIZEN. All other bits in this register should be maintained at the value last read (i.e., 0x3C04 or 0xBC04). **Example:** Write data 7C04h.
Write address 04h (This step is required for the Si4708/09 to reduce powerdown mode current). ■ **Set Register 4 [5:4] and [1:0] to 10b. All other bits in this register should be maintained at the value last read.** **Example: Write data 002Ah.**
Write address 02h (required). ■ Clear the DMUTE bit to enable mute. ■ Set the ENABLE bit high and DISABLE bit high to set the powerdown state. ■ After the DISABLE bit is set high, the device performs an internal powerdown sequence and then sets the ENABLE and DISABLE bits low. Setting the ENABLE bit directly to 0 will cause the device to partially powerdown. **Example:** Write data 0041h.

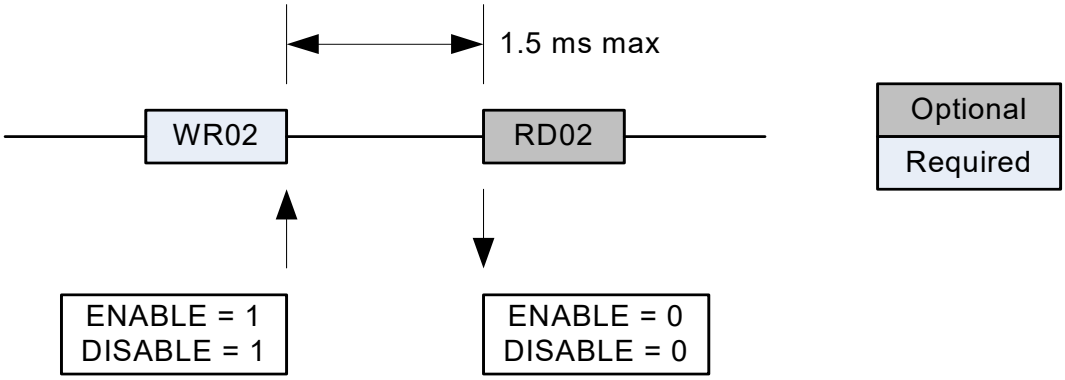


Figure 5. Powerdown Timing

3.2.2. XOSCEN-Crystal Oscillator Enable (Not available on Si4708/09)

The internal oscillator is not available on the Si4708/09. The Si4708/09-B requires a 32.768 kHz reference clock to the RCLK pin. Refer to the Si4708/09 datasheet for more information.

3.2.3. AHIZEN (07h.14)—Audio High-Z Enable

For information on audio high-Z enable, refer to Section 3.2.3 of “AN230: Si4700/01/02/03 Programming Guide."

3.2.4. GPIO1-General Purpose I/O 1 (Not available on Si4708/09)

General purpose I/O 1 is not available on the Si4708/09.

3.2.5. GPO (04h.3:2)/RDSIEN (04h.15)/STCIEN (04h.14)—General Purpose I/O, Interrupts

GPO can be programmed to four different states as shown in Table 5. When programmed as an interrupt, the device will generate interrupts based on the settings of RDSIEN and STCIEN. If RDSIEN is set a 5 ms interrupt pulse will be generated when RDS data is available. If STCIEN is set a 5 ms interrupt pulse will be generated upon completion of a SEEK or TUNE command. If both interrupts are enabled, the first interrupt after a SEEK or TUNE will be the STC interrupt. Subsequent interrupts will be RDS interrupts. This pin can also be used as a general purpose output or left unused. RDS is only available on the Si4709.

Table 5. GPO States

00	High impedance (default)
01	STC/RDS interrupt
10	Low output (GND level)
11	High output (VIO level)

3.2.6. GPIO3-General Purpose I/O 3 (Not available on Si4708/09)

General purpose I/O 3 is not available on the Si4708/09.

3.3. General Configuration Control Registers

For information on general configuration control registers, refer to Section 3.3 of “AN230: Si4700/01/02/03 Programming Guide."

3.4. Regional Configuration Control Registers

For information on regional configuration control registers, refer to Section 3.4 of “AN230: Si4700/01/02/03 Programming Guide."

3.5. End User Adjustable Control Registers

For information on end user adjustable control registers, refer to Section 3.5 of “AN230: Si4700/01/02/03 Programming Guide."

3.6. Seek Control Registers

For information on seek control registers, refer to Section 3.6 of “AN230: Si4700/01/02/03 Programming Guide."

3.7. Tune Control Registers

For information on tune control registers, refer to Section 3.7 of “AN230: Si4700/01/02/03 Programming Guide."

3.8. RDS/RBDS (Si4709 Only)

For information on RDS/RBDS, refer to Section 3.8 of “AN230: Si4700/01/02/03 Programming Guide." Note this section applies to the Si4709 in addition to the Si4701/03.

4. Programming with Commands

For information on programming with commands, refer to Section 4 of AN230 "Si4700/01/02/03 Programming Guide." Note this section applies to the Si4708/09 in addition to the Si4702/03 Rev C.

5. Command and Properties

For information on command and properties, refer to Section 5 of AN230 "Si4700/01/02/03 Programming Guide." Note this section applies to the Si4708/09 in addition to the Si4702/03 Rev C.

APPENDIX—SEEK ADJUSTABILITY AND SETTINGS

For information on seek adjustability and settings, refer to the Appendix in “AN230: Si4700/01/02/03 Programming Guide."

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