PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-AAS/13/7796
Dated 25 Apr 2013

High Speed CMOS Technology transfer from 5'' to 6'' in ST Singapore

Table 1. Change Implementation Schedule

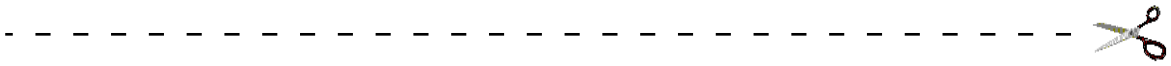
Forecasted implementation date for change	18-Apr-2013
Forecasted availability date of samples for customer	18-Apr-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	18-Apr-2013
Estimated date of changed product first shipment	25-Jul-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Waferfab process change
Reason for change	Production rationalization
Description of the change	Progressing on the activities related to high speed CMOS manufacturing processes, ST is glad to announce availability of 6 inches wafer production line, for AMS products in ST Ang Mo Kio (Singapore). Samples of M74HC4051RM13TR, M74HC04RM13TR, M74HC14RM13TR, M74HC151RM13TR, M74HC165RM13TR, M74HC4052RM13TR, M74HC4060RM13TR, M74HC4094RM13TR are available from now. Samples of other products will be available in the coming weeks upon customer request.
Change Product Identification	Date code & lot number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN AMS-AAS/13/7796**
Please sign and return to STMicroelectronics Sales Office	**Dated 25 Apr 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

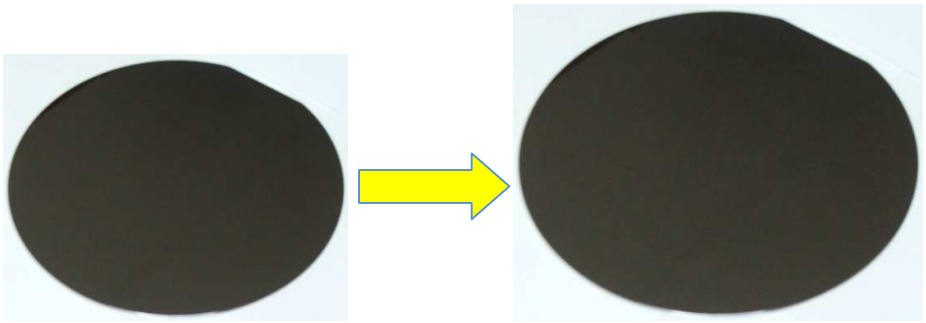
Name	Function
Grillo, Lionel	Marketing Manager
De marco, Alberto	Product Manager
Bugnard, Jean-Marc	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS-APD/13/7796

Analog, MEMS and Sensor Group

Wafer dimension change from 5 inches to 6 inches for High speed CMOS technology in ST Singapore



5 inches 6 inches

High speed CMOS

WHAT:

Progressing on the activities related to high speed CMOS manufacturing processes, ST is glad to announce availability of 6 inches wafer production line, for AMS products.

Material	Current process 5 inches	Modified process 6 inches	Comment
diffusion location	ST Ang Mo Kio (Singapore) ST AMJ9	ST Ang Mo Kio (Singapore) ST AMJ9	No change
Wafer dimension	5 inches	6 inches	
OCR (Optical charac-ter recognition)	NO	YES	Laser marking on wafer, which allow better traceability
Metallization	AlSi	AlSi	No change
Passivation	Pvapox/Nitride	Pvapox/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

For the complete list of part numbers affected by the change, please refer to the attached Product list.
Samples of M74HC4051RM13TR, M74HC04RM13TR, M74HC14RM13TR, M74HC151RM13TR, M74HC165RM13TR, M74HC4052RM13TR, M74HC4060RM13TR, M74HC4094RM13TR are available from now. Samples of other products will be available in the coming weeks upon customer request.

WHY:
To upgrade manufacturing line from 5 inches to 6 inches in order to improve customer service.

HOW:
The change that covers AMS (Analog, Mems & Sensors) products is qualified based on qualification plan here attached.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

WHEN:
Production in ST Singapore in 6 inches for AMS is forecasted week16 2013 for High Speed CMOS technology.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by datecode and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Change Qualification Plan

High speed CMOS transfer 5 to 6 inches

Test vehicle	
Product Lines:	*R595, Z460, Z494, Z451*
Product Families:	8 bit shift register without ouput latches (3 state), Single 8-Channel Analog Multiplexer/Demultiplexe, Single 8-Channel Analog Multiplexer/Demultiplexe
P/Ns:	*M74HC595YRM13TR, M74HC4060YRM13TR, M74HC4094YRM13TR, M74HC4051RM13TR*
Product Groups:	*AMS*
Product Divisions:	*Analog & Audio System*
Packages:	*SO16*
Silicon Process techn.:	*High speed CMOS*

Locations	
Wafer Diffusion Plants:	*ST Singapore*
EWS Plants:	*ST Singapore*
Assembly Plants:	*ST Bouskoura*
T&F Plants:	*ST Bouskoura*
Reliability Lab.:	*ST Catania*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	05-Apr-2013	15	JM Bugnard	First issue

Reference document :
REL-6043-055-13 / FLG-018, April 2013, author Giuseppe Failla and Angelo Basile Approved By Giovanni Presti
REL-6043-100.BSA.013.13, April 2013, author Giuseppe Failla and Angelo Basile Approved By Giovanni Presti
REL-6043-101.BSA.032-13, April 2013, author Giuseppe Failla and Angelo Basile Approved By Giovanni Presti

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
AEC-Q001	Guidelines for part average testing
AEC-Q003	Guidelines for Characterizing the Electrical Performance of IC Products
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 QUALIFICATION EVALUATION OVERVIEW

3.1 Objectives

Through this qualification plan, the high speed CMOS technology transfer is evaluated, to be diffused at ST Singapore in 6 inches instead of 5 inches.

3.2 Conclusion

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 CHANGE CHARACTERISTICS

4.1 Change description

Transfer of High Speed CMOS technology from 5 inches to 6 inches.

4.2 Change details

Material	Current process 5 inches	Modified process 6 inches	Comment
diffusion location	ST Ang Mo Kio (Singapore) ST AMJ9	ST Ang Mo Kio (Singapore) ST AMJ9	No change
Wafer dimension	5 inches	6 inches	
OCR (Optical character recognition)	NO	YES	Laser marking on wafer, which allow better traceability
Metallization	AlSi	AlSi	No change
Passivation	Pvapox/Nitride	Pvapox/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

4.3 Test vehicles description

	P/N *M74HC595YRM13TR*	P/N *M74HC4060YRM13TR*	P/N *M74HC4094YRM13TR*	P/N *M74HC4051RM13TR*
Wafer/Die fab. information				
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Technology	High speed CMOS	High speed CMOS	High speed CMOS	High speed CMOS
Process family	NHSFII_HSCMOS	NHSFII_HSCMOS	NHSFII_HSCMOS	NHSFII_HSCMOS
Die finishing back side	Lapped silicon	Lapped silicon	Lapped silicon	
Die size (microns)	2144x1412	2284x1794	1778x1274	1778x1726
Bond pad metallization layers	AlSi	AlSi	AlSi	AlSi
Passivation type	Pvapox+Nitride	Pvapox+Nitride	Pvapox+Nitride	Pvapox+Nitride
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1000	ASL1000	ASL1000	ASL1000
Assembly information				
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO16	SO16	SO16	SO16
Molding compound	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K
Frame material	Copper	Copper	Copper	Copper
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	Abklestick 8601-S25	Abklestick 8601-S25	Abklestick 8601-S25	Abklestick 8601-S25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Copper 1 mil	Copper 1 mil	Copper 1 mil	Copper 1 mil
Lead finishing process	Preplated frame	Preplated frame	Preplated frame	Preplated frame
Lead finishing/bump solder material	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu
Final testing information				
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	P/N	Process/ Package	Product Line	Comments
1	*M74HC595YRM13TR*	High speed CMOS/SO16	R595	Diffusion lot VW235NL92
2	*M74HC4060YRM13TR*	High speed CMOS/SO16	Z460	Diffusion lot VW241KPF
3	*M74HC4094YRM13TR*	High speed CMOS/SO16	Z494	Assy lot CZ2440LT01
4	*M74HC4051RM13TR*	High speed CMOS/TSSOP16	Z451	Diffusion lot VW241KPHE

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1	Lot 2	Lot 3	Lot4	
Die Oriented Tests										
HTB High Temp. Bias	N	JESD22 A-108	Tj = 125°C, BIAS		168H 1000H	0/77 0/77	0/77 0/77	(1)	0/77 0/77	
HTSL High Temp. Storage Life	N	JESD22 A-103	Ta = 150°C		168H 1000 H	0/45 0/45	0/45 0/45	(1)	0/45 0/45	
ELFR Early Life Failure Rate	N	AEC Q100 - 008	Ta=125°C		48H	0/800	0/800	(1)	0/800	
Package oriented test										
PC Preconditioning		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	(1)	Pass	MSL1
AC Auto Clave (Pressure Pot)	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H	0/77	0/77	(1)	0/77	
TC Temperature Cycling	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy 500cy	0/77 /077	0/77 /077	(1)	1/77 1/77	note(2)
THB Temperature Humidity Bias	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168H 500 H	0/77 0/77	0/77 0/77	(1)	0/77 0/77	
Other Tests										
ESD Electro Static Dis-charge	-	AEC Q101-001, 002 and 005	HBM		2kV	0/3	0/3	(1)	0/3	
			CDM			200V(0/3)	200V(0/3)	(1)	750V(0/3)	
			MM			750V(0/3)	1kV(0/3)	(1)		
LU Latch up	N	AEC Q100-004	LU			0/12	0/12	(1)		

(1) Electrical characterization only
(2) 1 reject in thermal cycling due to broken stitch, handling issue not linked with present diffusion qualification.

6 ANNEXES

6.1 Comparison Data Results

6.1.1 Electrical Data

Part Number: *M74HC4060YRM13TR (Final test)*

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	High Level Output Voltage (Q Output)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		

Parameter	Results						
			Before Change		After Change		Note
test parameter	Out	Unit	Avg	Cpk	Avg	Cpk	Note
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q12	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q13	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q14	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q6	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q5	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q7	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q4	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q9	V	1.99	>2	1.99	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q8	V	1.99	>2	2.00	>2	conform
VOH (High Level Output Voltage) at Vcc=2V Iout=-20uA	Q10		1.99	>2	2.00	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	Q12	V	4.32	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	Q13	V	4.32	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	Q14	V	4.31	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	Q6	V	4.30	>2	4.27	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	Q5	V	4.30	>2	4.26	>2	conform
VOH (High Level Output Voltage at Vcc=4.5V Iout=-4mA	Q7	V	4.30	>2	4.27	>2	conform
VOH (High Level Output Voltage)) at Vcc=4.5V Iout=-4mA	Q4	V	4.30	>2	4.26	>2	conform
VOH (High Level Output Voltage)) at Vcc=4.5V Iout=-4mA	Q9	V	4.31	>2	4.27	>2	conform
VOH (High Level Output Voltage)) at Vcc=4.5V Iout=-4mA	Q8	V	4.31	>1.66	4.26	>1.66	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	Q10	V	4.31	>2	4.27	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q12	V	5.85	>2	5.82	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q13	V	5.85	>2	5.82	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q14	V	5.84	>2	5.82	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q6	V	5.84	>2	5.81	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q5	V	5.84	>2	5.80	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q7	V	5.83	>2	5.81	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	Q4	V	5.83	>2	5.80	>2	conform
VOH (High Level Output Voltage)) at Vcc=6V Iout=-5.2mA	Q9	V	5.83	>2	5.80	>2	conform
VOH (High Level Output Voltage) (Q Output) at Vcc=6V Iout=-5.2mA	Q8	V	5.84	>2	5.80	>2	conform
VOH (High Level Output Voltage) (Q Output) at Vcc=6V Iout=-5.2mA	Q10	V	5.84	>2	5.81	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage (Q Output)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	

Parameter	Results						
			Before Change		After Change		
test parameter	Out	Unit	Avg	Cpk	Avg	Cpk	Note
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 1	mV	14.49	>2	49.72	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 2	mV	0.72	>2	2.60	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 3	mV	0.13	>2	1.47	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 4	mV	0.50	>2	1.64	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 5	mV	0.14	>2	1.60	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 6	mV	0.46	>2	1.42	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 7	mV	0.60	>2	1.60	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 13	mV	0.64	>2	1.41	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 14	mV	0.77	>2	1.76	>2	conform
VOL (Low Level Output Voltage) at Vcc=2V Iout=20uA	Vol pin 15	mV	0.30	>2	1.71	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 1	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 2	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 3	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 4	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 5	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 6	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 7	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 13	V	0.14	>2	0.16	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 14	V	0.14	|2	0.16	|2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	Vol pin 15	V	0.14	>2	0.17	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 1	mV	140.77	>2	158.64	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 2	mV	140.39	>2	155.65	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 3	mV	135.53	>2	156.09	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 4	mV	135.00	>2	160.77	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 5	mV	133.22	>2	152.94	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 6	mV	132.22	>2	153.47	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 7	mV	134.56	>2	152.37	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 13	mV	137.00	>2	159.62	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 14	mV	135.55	>2	154.01	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	Vol pin 15	mV	138.80	>2	165.62	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	µA

Parameter	Unit	Results				Note
		Before Change		After Change		
test parameter		Avg	Cpk	Avg	Cpk	
IL (Input Leakage current)	nA	3.07	>2	2.3	>2	conform
IL (Input Leakage current)	nA	5.51	>2	2.8	>2	conform
IL (Input Leakage current)	nA	18.06	>2	12.9	>2	conform
IL (Input Leakage current)	nA	5.99	>2	4.2	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	µA

Parameter	Unit	Results				Note
		Before Change		After Change		
test parameter		Avg	Cpk	Avg	Cpk	
ICC1 (Quiescent Supply Current) Vcc=6V	uA	0.21	>2	0.13	>2	conform
ICC2 (Quiescent Supply Current) Vcc=6V	uA	0.02	>2	0.01	>2	conform
ICC3 (Quiescent Supply Current) Vcc=6V	uA	0.27	>2	0.30	>2	conform
ICC4 (Quiescent Supply Current) Vcc=6V	uA	0.00	>2	0.04	>2	conform

Part number: M74HC4094YRM13TR

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		

Parameter	Results						
			Before Change		After Change		Note
test parameter	Pins	Unit	Avg	Cpk	Avg	Cpk	
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 4	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH Pin 5	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 6	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 7	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 14	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 13	V	4.30	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 12	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 11	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 10	V	4.29	>2	4.28	>2	conform
VOH (High Level Output Voltage) at Vcc=4.5V Iout=-4mA	VoH pin 9	V	4.30	>2	4.29	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 4	V	5.78	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 5	V	5.78	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 6	V	5.79	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 7	V	5.78	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 14	V	5.78	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 13	V	5.79	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 12	V	5.78	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 11	V	5.78	>2	5.77	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 10	V	5.78	>2	5.78	>2	conform
VOH (High Level Output Voltage) at Vcc=6V Iout=-5.2mA	VoH pin 9	V	5.79	>2	5.78	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	

Parameter	Results						
		Unit	Before Change		After Change		Note
test parameter	Pins		Avg	Cpk	Avg	Cpk	
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 4	mV	151	>2	151	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 5	mV	150	>2	151	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 6	mV	149	>2	150	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 7	mV	148	>2	150	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 14	mV	153	>2	154	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 13	mV	152	>2	154	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 12	mV	152	>2	153	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 11	mV	152	>2	152	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 10	mV	152	>2	153	>2	conform
VOL (Low Level Output Voltage) at Vcc=4.5V Iout=4mA	VoL pin 9	mV	152	>2	158	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 4	mV	152	>2	151	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 5	mV	150	>2	151	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 6	mV	149	>2	149	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 7	mV	148	>2	149	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 14	mV	153	>2	155	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 13	mV	153	>2	154	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 12	mV	152	>2	154	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 11	mV	152	>2	153	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 10	mV	151	>2	153	>2	conform
VOL (Low Level Output Voltage) at Vcc=6V Iout=5.2mA	VoL pin 9	mV	152	>2	158	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA

Parameter	Results						
		Unit	Before Change		After Change		Note
test parameter	Pins		Avg	Cpk	Avg	Cpk	
IL (Input Leakage current)	In Leak High PIN1	nA	1.3	>2	3.3	>2	conform
IL (Input Leakage current)	In Leak HighPIN2	nA	0.4	>2	0.6	>2	conform
IL (Input Leakage current)	In Leak High PIN3	nA	1.1	>2	1.7	>2	conform
IL (Input Leakage current)	In Leak High PIN15	nA	3.9	>2	4.3	>2	conform
IL (Input Leakage current)	In Leak Low PIN1	nA	2.3	>2	5.5	>2	conform
IL (Input Leakage current)	In Leak Low PIN2	nA	4.4	>2	3.6	>2	conform
IL (Input Leakage current)	In Leak Low PIN3	nA	4.0	>2	4.2	>2	conform
IL (Input Leakage current)	In Leak Low PIN15	nA	5.9	>2	9.0	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	µA

Parameter	Results						
			Before Change		After Change		Note
test parameter	Pins	Unit	Avg	Cpk	Avg	Cpk	
ICC (Quiescent Supply Current) Vcc=6V	Icc @6V	uA	0.14	>2	0.12	>2	conform

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{OZ}	High Impedance Output Leakage Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			± 0.5		± 5		± 10	µA

Parameter	Results						
			Before Change		After Change		Note
test parameter	Pins	Unit	Avg	Cpk	Avg	Cpk	
IOZ (High Impedance Output Leakage Current)	IOZH Q1	nA	23.17	>2	28.62	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q2	nA	2.5	>2	2.6	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q3	nA	0.9	>2	0.5	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q4	nA	2.1	>2	2.5	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q5	nA	7.4	>2	14.1	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q6	nA	2.2	>2	2.8	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q7	nA	2.3	>2	3.0	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZH Q8	nA	1.2	>2	1.2	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q1	nA	6	>2	6	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q2	nA	2	>2	3	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q3	nA	3	>2	1	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q4	nA	0	>2	1	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q5	nA	8	>2	0	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q6	nA	0	>2	2	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q7	nA	0	>2	2	>2	conform
IOZ (High Impedance Output Leakage Current)	IOZL Q8	nA	1	>2	1	>2	conform

Part number *M74HC4051RM13TR*

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
					Min	Typ	Max	Min	Max	Min	Max	
R_{ON}	ON resistance	4.5	GND	$V_I = V_{IHC}$ or V_{ILC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$		85	180		225		270	W
		4.5	-4.5			55	120		150		180	
		6.0	-6.0			50	100		125		150	
		2.0	GND	$V_I = V_{IHC}$ or V_{ILC} $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O} \leq 2$ mA		150						
		4.5	GND			70	150		190		230	
		4.5	-4.5			50	100		125		150	
		6.0	-6.0			45	80		100		120	

Parameter	Unit	Before Change		After Change		Note
test parameter		Avg	Cpk	Avg	Cpk	
RON Vcc GND	OHM	79.25	>2	76.54	>2	conform
RON STEP	OHM	97.28	>2	90.35	>2	conform

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
					Min	Typ	Max	Min	Max	Min	Max	
I_{OFF}	Input/output leakage current (switch off)	6.0	GND	$V_{OS} = V_{CC}$ or GND V_{IS} = GND or V_{CC} $V_I = V_{ILC}$ or V_{IHC}			±0.06		±0.6		±1.2	µA
		6.0	-6.0				±0.1		±1		±2	

Parameter	Unit	Before Change		After Change		Note
test parameter		Avg	Cpk	Avg	Cpk	
IOFF3_pin13	nA	-4.64	>2	-32.19	>2	conform
IOFF3_pin14	nA	7.30	>2	-14.21	>2	conform
IOFF3_pin15	nA	-5.36	>2	-46.21	>2	conform
IOFF3_pin12	nA	-4.30	>2	-29.06	>2	conform
IOFF3_pin1	nA	-5.33	>2	-34.57	>2	conform
IOFF3_pin5	nA	-5.37	>2	-33.66	>2	conform
IOFF3_pin2	nA	-4.86	>2	-28.10	>2	conform
IOFF3_pin4	nA	-4.59	>2	-27.77	>2	conform
IOFF7_pin3	nA	0.01	>2	-4.15	>2	conform
IOFF6_pin13	nA	0.67	>2	15.21	>2	conform
IOFF6_pin14	nA	1.76	>2	26.35	>2	conform
IOFF6_pin15	nA	1.00	>2	17.30	>2	conform
IOFF6_pin12	nA	1.60	>2	29.86	>2	conform
IOFF6_pin1	nA	-4.04	>2	-23.05	>2	conform
IOFF6_pin5	nA	-4.20	>2	-22.87	>2	conform
IOFF6_pin2	nA	-4.36	>2	-24.09	>2	conform
IOFF6_pin4	nA	-4.46	>2	-23.65	>2	conform
IOFF10_pin3	nA	4.66	>2	24.67	>2	conform

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
					Min	Typ	Max	Min	Max	Min	Max	
I_I	Input leakage current	6.0	GND	$V_I = V_{CC}$ or GND			±0.1		±0.1		±1	µA

Parameter						
test parameter	Unit	Before Change		After Change		Note
		Avg	Cpk	Avg	Cpk	
ILH_Inp A	nA	3.76	>1.3	31.52	>2	conform
ILH_Inp B	nA	-2.13	>2	20.35	>2	conform
ILH_Inp_C	nA	5.46	>2	28.00	>2	conform
ILH_Inp INH	nA	7.43	>2	13.27	>2	conform
ILL_Inp A	nA	-5.01	>2	-17.41	>2	conform
ILL_Inp_B	nA	-3.12	>2	-10.08	>2	conform
ILL_Inp_C	nA	-6.32	>2	-19.65	>2	conform
ILL_Inp_INH	nA	6.56	>2	6.52	>2	conform

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
					Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	Quiescent supply current	6.0	GND	$V_I = V_{CC}$ or GND			4		40		80	µA
		6.0	-6.0				8		80		160	

Parameter							
test parameter		unit	Before Change		After Change		Note
			Avg	Cpk	Avg	Cpk	
Icc(VEE_HIGH)	VI=Vih	uA	-0.01	>2	-0.01	>2	conform
Icc(VEE_LOW)	VI=Vil	uA	-0.01	>2	-0.01	>2	conform
Icc(VEE_HIGH)	VI=Vih	uA	-0.01	>2	0.06	>2	conform
Icc(VEE_LOW)	VI=Vil	uA	0.00	>2	0.07	>2	conform

Conclusion: New version in line with requirements.

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
PTC Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not uinduced by fixturing or handling.
EV External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,…).
LI Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
WBP Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
WBS Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
DS Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
PD Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
SD Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Public Products List

PCN Title : High Speed CMOS Technology transfer from 5'' to 6'' in ST Singapore
PCN Reference : AMS-AAS/13/7796
PCN Created on : 30-APR-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

74H1G66STR	M74HC00B1R	M74HC00RM13TR
M74HC00TTR	M74HC02B1R	M74HC02RM13TR
M74HC02TTR	M74HC03RM13TR	M74HC03TTR
M74HC04B1R	M74HC04RM13TR	M74HC04TTR
M74HC08B1R	M74HC08RM13TR	M74HC08TTR
M74HC107RM13TR	M74HC109RM13TR	M74HC10RM13TR
M74HC123B1R	M74HC123TTR	M74HC125B1R
M74HC125RM13TR	M74HC125TTR	M74HC126RM13TR
M74HC126TTR	M74HC132B1R	M74HC132RM13TR
M74HC132TTR	M74HC138B1R	M74HC138RM13TR
M74HC138TTR	M74HC139B1R	M74HC139RM13TR
M74HC139TTR	M74HC148B1R	M74HC148RM13TR
M74HC148TTR	M74HC14B1R	M74HC14RM13TR
M74HC14TTR	M74HC151B1R	M74HC151RM13TR
M74HC151TTR	M74HC153TTR	M74HC157B1R
M74HC157RM13TR	M74HC160RM13TR	M74HC161B1R
M74HC161RM13TR	M74HC161TTR	M74HC163RM13TR
M74HC164B1R	M74HC164RM13TR	M74HC164TTR
M74HC165B1R	M74HC165RM13TR	M74HC165TTR
M74HC174B1R	M74HC174RM13TR	M74HC174TTR
M74HC175B1R	M74HC175RM13TR	M74HC175TTR
M74HC191RM13TR	M74HC20RM13TR	M74HC221B1R
M74HC221RM13TR	M74HC238B1R	M74HC238RM13TR
M74HC238TTR	M74HC240RM13TR	M74HC241RM13TR
M74HC244RM13TR	M74HC244TTR	M74HC245RM13TR
M74HC245TTR	M74HC251B1R	M74HC251RM13TR
M74HC251TTR	M74HC253RM13TR	M74HC257B1R
M74HC257RM13TR	M74HC259B1R	M74HC259RM13TR
M74HC259TTR	M74HC266RM13TR	M74HC273RM13TR
M74HC273TTR	M74HC27RM13TR	M74HC27TTR
M74HC280RM13TR	M74HC283RM13TR	M74HC299RM13TR
M74HC32B1R	M74HC32RM13TR	M74HC32TTR
M74HC365B1R	M74HC365RM13TR	M74HC365TTR
M74HC367B1R	M74HC367RM13TR	M74HC367TTR
M74HC368B1R	M74HC368RM13TR	M74HC373RM13TR

Public Products List

PCN Title : High Speed CMOS Technology transfer from 5'' to 6'' in ST Singapore
PCN Reference : AMS-AAS/13/7796
PCN Created on : 30-APR-2013

Subject : Public Products List (Contd.)

ST COMMERCIAL PRODUCT

M74HC373TTR
M74HC374RM13TR
M74HC377RM13TR
M74HC390B1R
M74HC390RM13TR
M74HC393B1R
M74HC393RM13TR
M74HC393TTR
M74HC4017B1R
M74HC4017RM13TR
M74HC4020B1R
M74HC4020RM13TR
M74HC4024B1R
M74HC4024RM13TR
M74HC4040B1R
M74HC4040RM13TR
M74HC4040TTR
M74HC4049B1R
M74HC4049RM13TR
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M74HC4050RM13TR
M74HC4050TTR
M74HC4051B1R
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M74HC4051TTR
M74HC4052B1R
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M74HC4052TTR
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M74HC4060B1R
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M74HC4060TTR
M74HC4066B1R
M74HC4066RM13TR
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M74HC4075B1R
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M74HC4094B1R
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M74HC4316B1R
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M74HC4518B1R
M74HC4520B1R
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M74HC540RM13TR
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M74HC573TTR
M74HC574RM13TR
M74HC574TTR
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M74HC7266B1R
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M74HCT04RM13TR
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M74HCT132B1R
M74HCT132TTR
M74HCT138RM13TR
M74HCT14B1R
M74HCT14RM13TR
M74HCT14TTR
M74HCT157RM13TR
M74HCT244RM13TR
M74HCT244TTR
M74HCT273RM13TR

Public Products List

PCN Title : High Speed CMOS Technology transfer from 5'' to 6'' in ST Singapore
PCN Reference : AMS-AAS/13/7796
PCN Created on : 30-APR-2013

Subject : Public Products List (Contd.)

ST COMMERCIAL PRODUCT

M74HCT32B1R
M74HCT32RM13TR
M74HCT367RM13TR
M74HCT373RM13TR
M74HCT373TTR
M74HCT374RM13TR
M74HCT4051RM13TR
M74HCT4051TTR
M74HCT4053RM13TR
M74HCT4053TTR
M74HCT540RM13TR
M74HCT541RM13TR
M74HCT573RM13TR
M74HCT573TTR
M74HCT574RM13TR
M74HCT574TTR
M74HCT640RM13TR
M74HCT652RM13TR
M74HCT7007RM13TR
M74HCT74RM13TR
M74HCT74TTR
M74HCU04RM13TR
M74HCU04TTR
M74HC133RM13TR
M74HC133B1R

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