

PM5376 TSE-Nx160

Transmission Switch Element

Released Product Brief



Features

Switching Capacity

- Implements a 64-port memory switch fabric with STS-1/AU-3 switching granularity and scaling capability in a single device.
- With a set of four devices, implements a 640G 256-port single-stage switch fabric. With a set of two devices, implements a 320G 128-port single stage switch fabric.
- Supports non-blocking anycast switching in all single stage configurations.
- Supports fabric capacities greater than 640G using multi-stage fabrics.
- Provides two pages of connection memory with software and hardware controlled hitless page swaps at frame boundaries.
- Supports trunk conditioning on a per port, per egress grain basis for AIS and UNEQ insertion.
- Propagation of unselected ingress grains in the device can be optionally disabled to reduce device power consumption.

Switch Port Configuration

- Each ingress and egress link can be individually configured to support STS-48 or STS-12 equivalent flows using SONET scrambling over RASIO™ links.
- Interfaces to industry standard components via 622 Mbit/s or 2.488 Gbit/s configured ports.
- Interfaces to the TBS 2488 and the ARROW family of framers for di-bit, nibble, or byte switching.

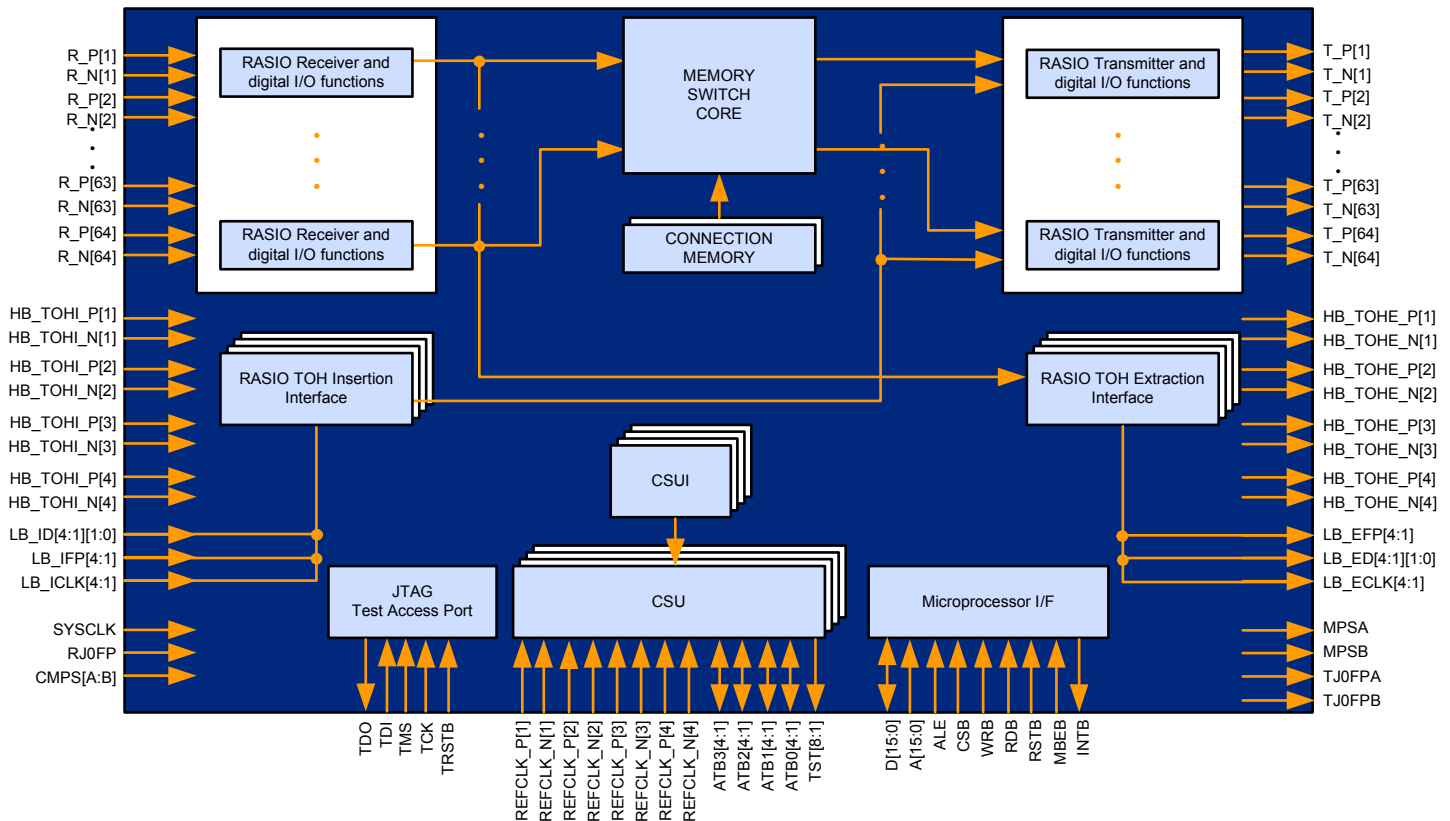
Centralized Overhead Accessibility

- Provides a high bandwidth interface with insert and extract access to all TOH bytes from all ports.
- Provides a clock and data interface where the number of extracted and inserted TOH bytes is limited to 99 bytes per port selected for each ingress port.

Implements the ESSI Frame Layer

- Provides in-service link verification via bit interleaved parity (BIP-8) monitoring of the B1 byte.
- Optionally generates standard B1 byte on egress flows.
- Provides out of frame alignment status information for each ingress port.
- Provides per link SONET-framed and unframed PRBS-23 generation and monitoring for off-line link verification.

Block Diagram



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Global Frame Synchronization

- Provides two independent frame alignment planes.
- Supports frame synchronization using ESSi smart framing or a global frame pulse input signal.
- Compensates for differences in frame boundary arrival times between ingress ports using FIFOs and device level software configurable delay registers.

I/O and General

- Robust signal integrity over high speed links using PMC-Sierra's RASIO CML I/O for high speed serial ingress, egress, and transport overhead links. RASIO links are E-LVDS compatible.
- Programmable pre-emphasis on transmit, equalization on receiver, and supports both AC and DC coupling.
- Low power 1.2V CMOS core with 2.5V or 3.3V CMOS / TTL selectable digital inputs and outputs.

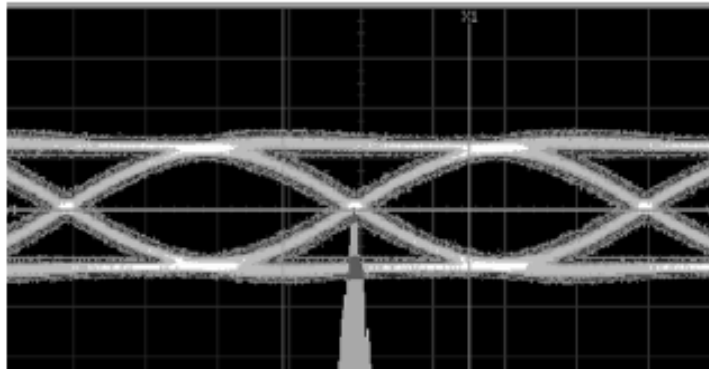
- Low power consumption.
- Generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board testing.
- 1152-FCBGA package
- Includes proprietary Transient Current Demand Management (TCDM) technology that simplifies power supply design.

Applications

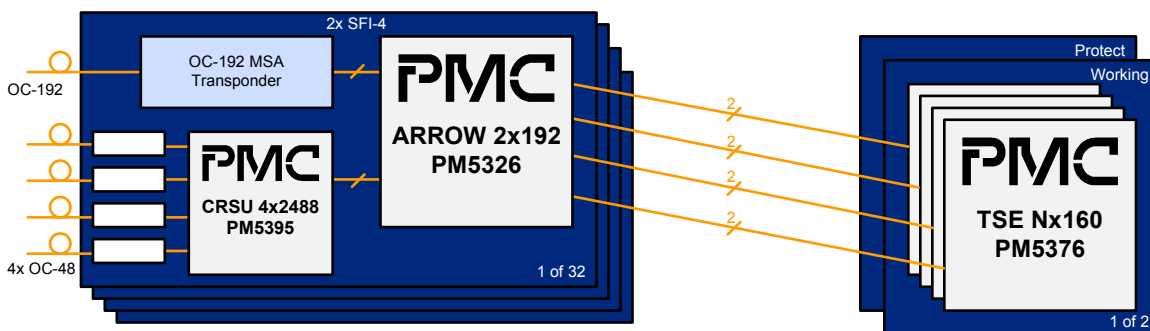
- Optical Cross-connects.
- Multi-service Provisioning Platforms.
- SONET/SDH Digital Cross-connects.
- SONET/SDH Add/Drop Multiplexers.
- SONET/SDH Terminal Multiplexers.

Typical Result of RASIO 40-inch Reach Using FR-4

Scale: 100ps/div.; 200mV/div



Typical Application: 640G Cross-Connect with 20G Line Cards



Further Resources

Technology Webpage

www.pmcs.com/products/optical_network/sonet_sdh/

Technical Documentation

www.pmcs.com/resources/downloads_support.html

About PMC

PMC (Nasdaq:PMCS) is the semiconductor innovator transforming networks that connect, move and store digital content. Building on a track record of technology leadership, we are driving innovation across storage, optical and mobile networks. Our highly integrated solutions increase performance and enable next generation services to accelerate the network transformation. For more information visit www.pmcs.com.

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