

# SN65LBC180-Q1 LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIR

SGLS251A – JULY 2004 – REVISED JUNE 2008

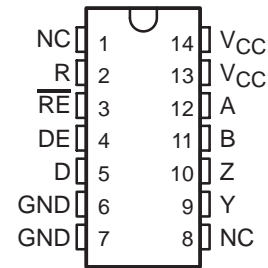
- Qualified for Automotive Applications
- Designed for High-Speed Multipoint Data Transmission Over Long Cables
- Operate With Pulse Durations as Low as 30 ns
- Low Supply Current . . . 5 mA Max
- Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)
- 3-State Outputs for Party-Line Buses
- Common-Mode Voltage Range of -7 V to 12 V
- Thermal Shutdown Protection Prevents Driver Damage From Bus Contention
- Positive and Negative Output Current Limiting
- Pin Compatible With the SN75ALS180

## description

The SN65LBC180 differential driver and receiver pair is a monolithic integrated circuit designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. It is a balanced, or differential, voltage mode device that meets or exceeds the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). The device is designed using TI's proprietary LinBiCMOS™ with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

The SN65LBC180 combines a differential line driver and receiver with 3-state outputs and operates from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off ( $V_{CC} = 0$ ). This part features a wide common-mode voltage range making it suitable for point-to-point or multipoint data-bus applications.

D PACKAGE  
(TOP VIEW)



NC—No internal connection

## Function Tables

### DRIVER

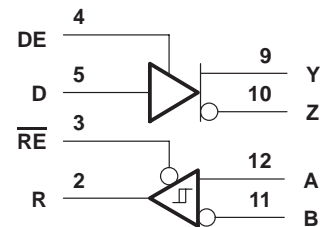
INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

### RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open circuit	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

## logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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### description/ordering information (continued)

#### ORDERING INFORMATION†

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tape and reel	SN65LBC180IDRQ1	LBC180Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

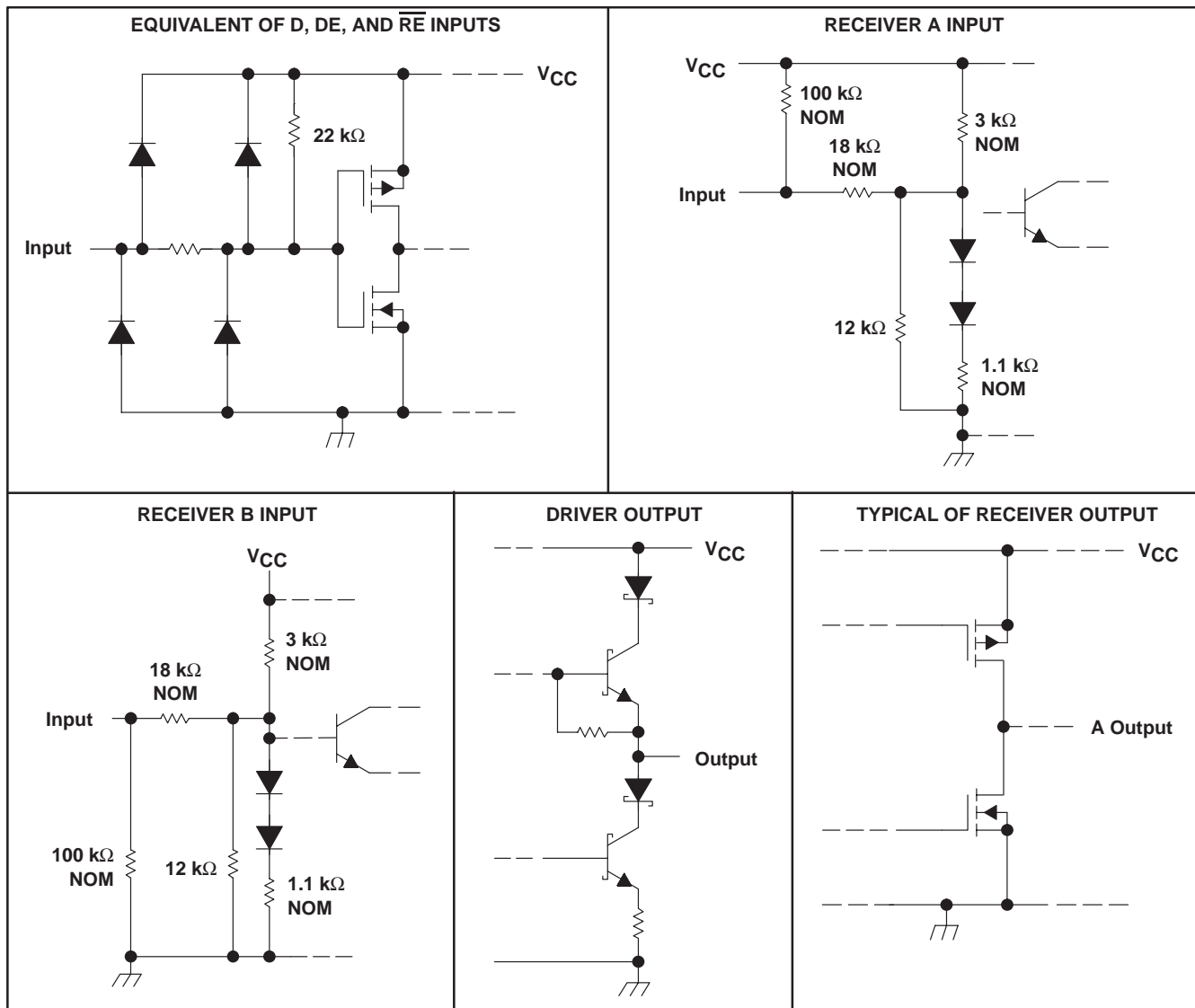


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## schematics of inputs and outputs



# SN65LBC180-Q1

## LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIR

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 7 V
Input voltage range, $V_I$ (A, B)(see Note 1)	–10 V to 15 V
Voltage range at D, R, DE, $\overline{RE}$ (see Note 1)	–0.3 V to $V_{CC} + 0.5$ V
Continuous total power dissipation (see Note 2)	Internally limited
Total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.  
 2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $V_{ID}$		–6‡		6	V
Voltage at any bus terminal (separately or common mode), $V_O$ , $V_I$ , or $V_{IC}$	A, B, Y, or Z	–7‡		12	V
High-level output current, $I_{OH}$	Y or Z			–60	mA
	R			–8	
Low-level output current, $I_{OL}$	Y or Z			60	mA
	R			8	
Operating free-air temperature, $T_A$		–40		85	°C

‡ The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.



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## LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIR

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### DRIVER SECTION

#### electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
$ V_{OD} $	Differential output voltage magnitude (see Note 3)	$R_L = 54 \Omega$ ,	See Figure 1	1.1	2.5	5	V
		$R_L = 60 \Omega$ ,	See Figure 2	1.1	2	5	
$\Delta V_{OD} $	Change in magnitude of differential output voltage (see Note 4)	See Figures 1 and 2				$\pm 0.2$	V
$V_{OC}$	Common-mode output voltage			1	2.5	3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage (see Note 4)	$R_L = 54 \Omega$ ,	See Figure 1			$\pm 0.2$	V
$I_O$	Output current with power off	$V_{CC} = 0$ ,	$V_O = -7 \text{ V to } 12 \text{ V}$			$\pm 100$	$\mu\text{A}$
$I_{OZ}$	High-impedance-state output current	$V_O = -7 \text{ V to } 12 \text{ V}$				$\pm 100$	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_I = 2.4 \text{ V}$				-100	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0.4 \text{ V}$				-100	$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$-7 \text{ V} \leq V_O \leq 12 \text{ V}$				$\pm 250$	mA
$I_{CC}$	Supply current	Receiver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

- NOTES: 3. The minimum  $V_{OD}$  specification of the SN65LBC180 may not fully comply with ANSI RS-485 at operating temperatures below  $0^\circ\text{C}$ . System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.
4.  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in the steady-state magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

#### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54 \Omega$ ,	See Figure 3	7	12	18	ns
$t_{t(OD)}$	Differential output transition time			5	10	20	ns
$t_{PZH}$	Output enable time to high level	$R_L = 110 \Omega$ ,	See Figure 4			35	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110 \Omega$ ,	See Figure 5			35	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110 \Omega$ ,	See Figure 4			50	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110 \Omega$ ,	See Figure 5			35	ns

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### RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

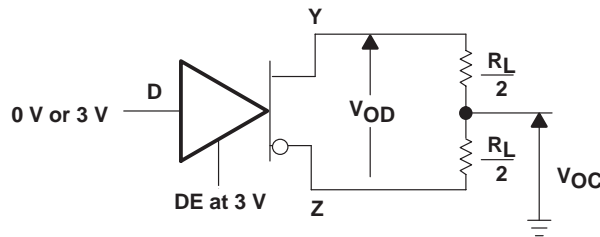
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$				0.2	V
$V_{IT-}$	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$		-0.2			V
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				45		mV
$V_{IK}$	Enable-input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 200 \text{ mV}$ ,	$I_{OH} = -8 \text{ mA}$	3.5	4.5		V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200 \text{ mV}$ ,	$I_{OL} = 8 \text{ mA}$		0.3	0.5	V
$I_{OZ}$	High-impedance-state output current	$V_O = 0 \text{ V to } V_{CC}$				$\pm 20$	$\mu\text{A}$
$I_{IH}$	High-level enable-input current	$V_{IH} = 2.4 \text{ V}$				-50	$\mu\text{A}$
$I_{IL}$	Low-level enable-input current	$V_{IL} = 0.4 \text{ V}$				-100	$\mu\text{A}$
$I_I$	Bus input current	$V_I = 12 \text{ V}$ ,	$V_{CC} = 5 \text{ V}$ ,		0.7	1	mA
		Other input at 0 V					
		$V_I = 12 \text{ V}$ ,	$V_{CC} = 0 \text{ V}$ ,				
		Other input at 0 V					
		$V_I = -7 \text{ V}$ ,	$V_{CC} = 5 \text{ V}$ ,		-0.5	-0.8	
		Other input at 0 V					
		$V_I = -7 \text{ V}$ ,	$V_{CC} = 0 \text{ V}$ ,		-0.5	-0.8	
		Other input at 0 V					
$I_{CC}$	Supply current	Driver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

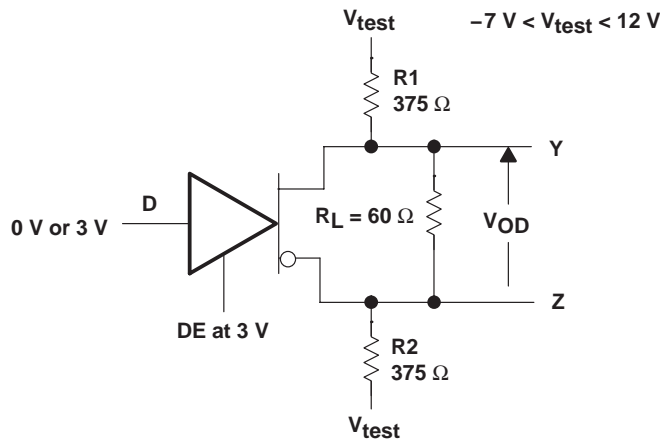
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$ ,	See Figure 6	11	22	33	ns
$t_{PLH}$	Propagation delay time, low- to high-level output			11	22	33	ns
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )			3	6		ns
$t_t$	Transition time			5	8		ns
$t_{PZH}$	Output enable time to high level	See Figure 7				35	ns
$t_{PZL}$	Output enable time to low level					30	ns
$t_{PHZ}$	Output disable time from high level					35	ns
$t_{PLZ}$	Output disable time from low level					30	ns



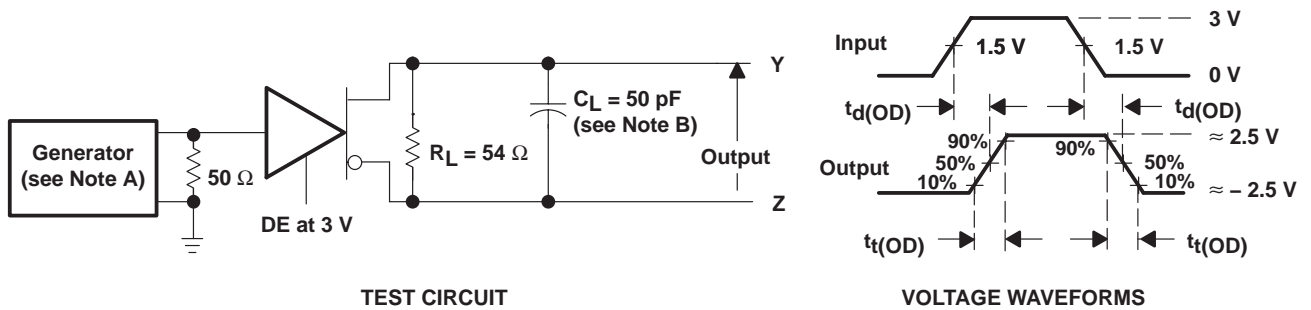
**PARAMETER MEASUREMENT INFORMATION**



**Figure 1. Differential and Common-Mode Output Voltages**



**Figure 2. Driver  $V_{OD}$  Test Circuit**



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms**

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### PARAMETER MEASUREMENT INFORMATION

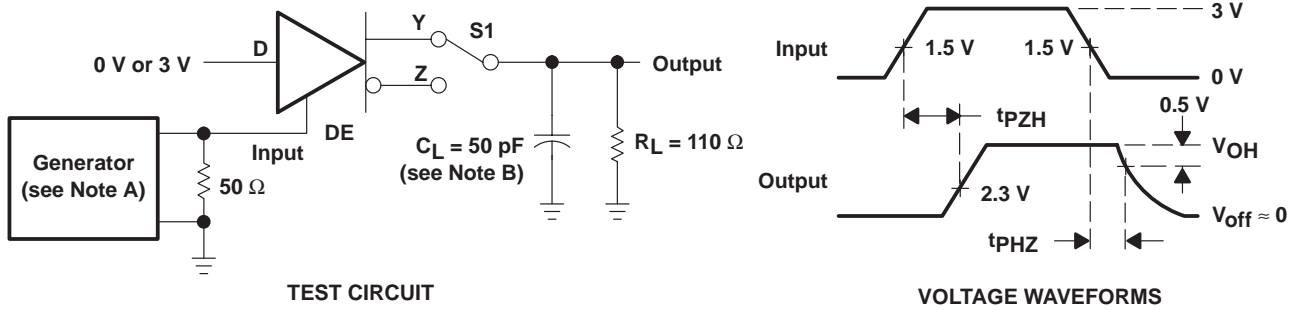


Figure 4. Driver Test Circuit and Enable and Disable Time Waveforms

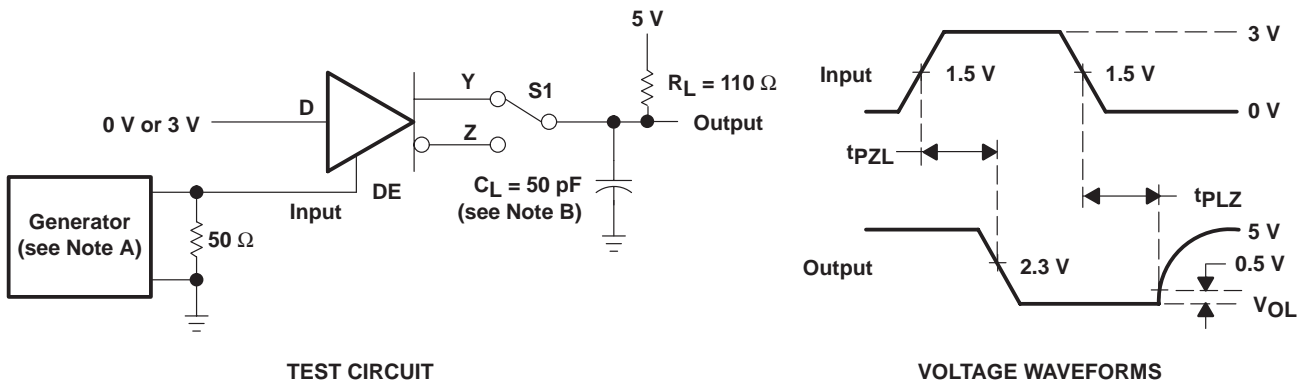
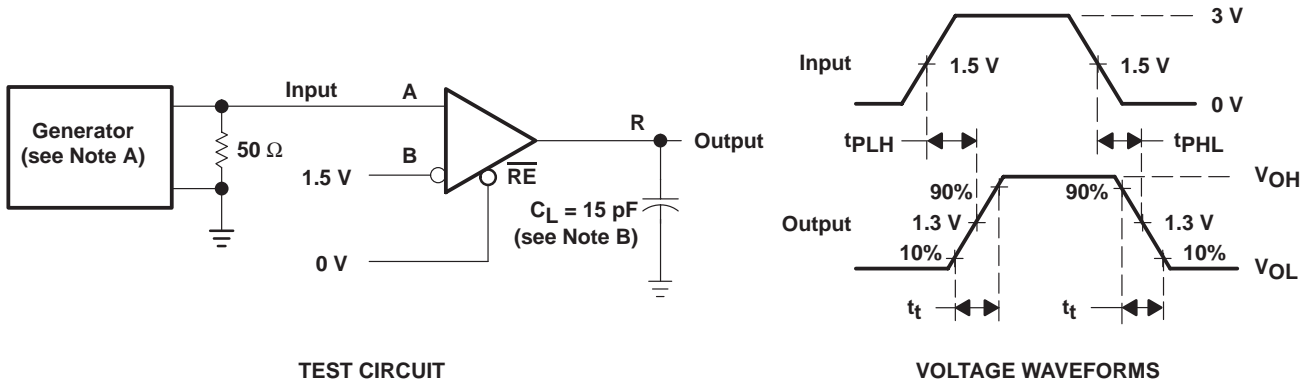


Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_0 = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms

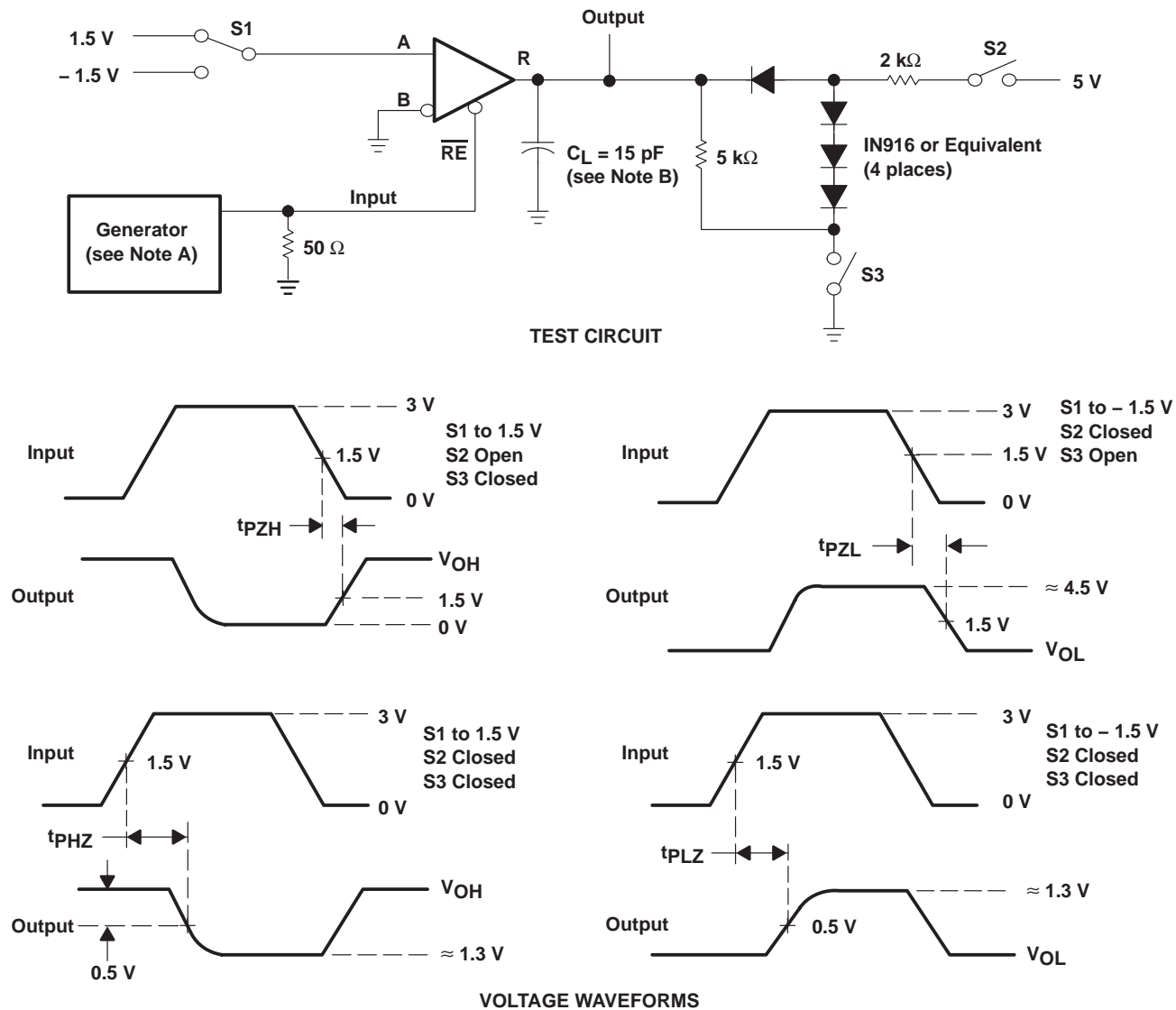


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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 7. Receiver Output Enable and Disable Times**

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## LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIR

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### TYPICAL CHARACTERISTICS

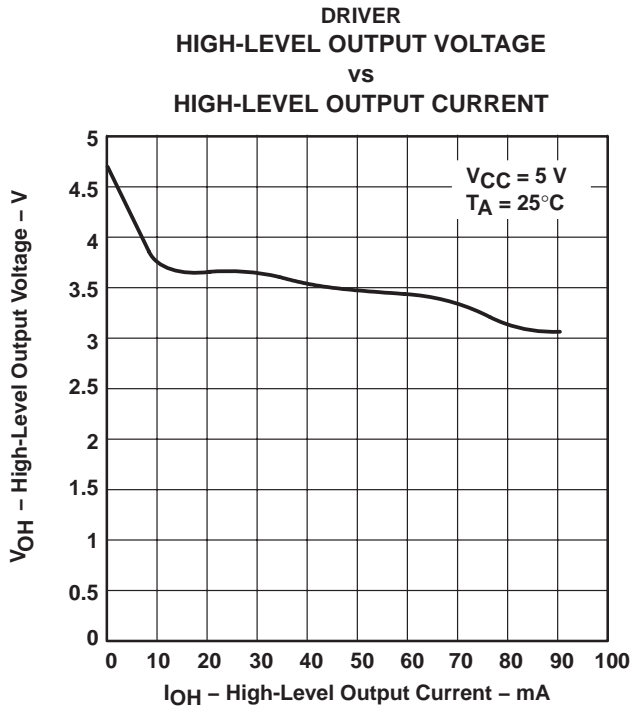


Figure 8

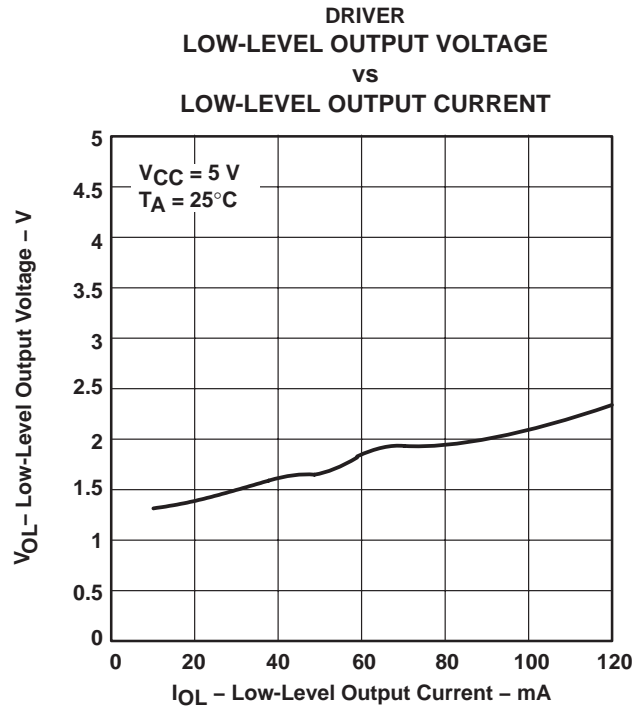


Figure 9

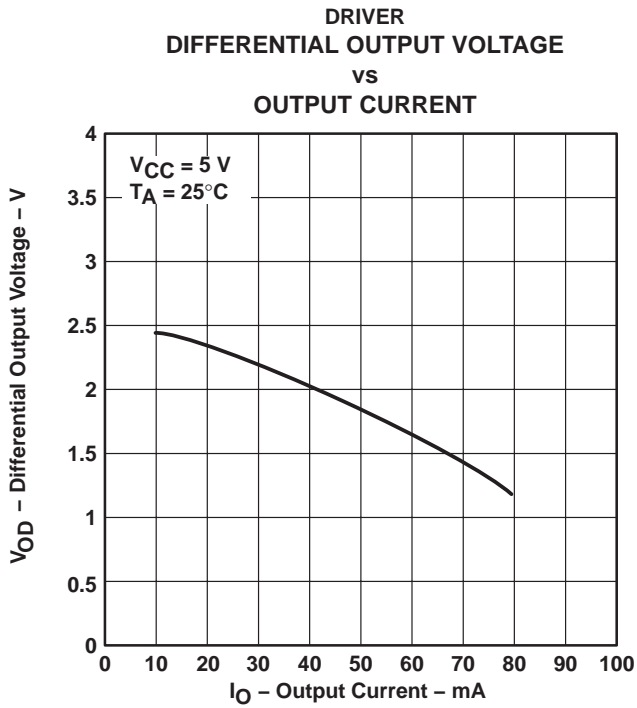


Figure 10

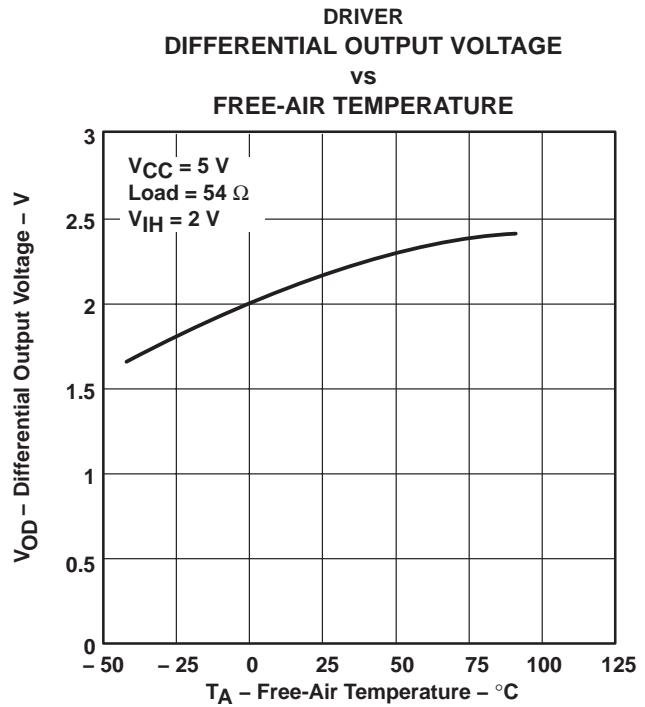


Figure 11



# SN65LBC180-Q1

## LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIR

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### TYPICAL CHARACTERISTICS

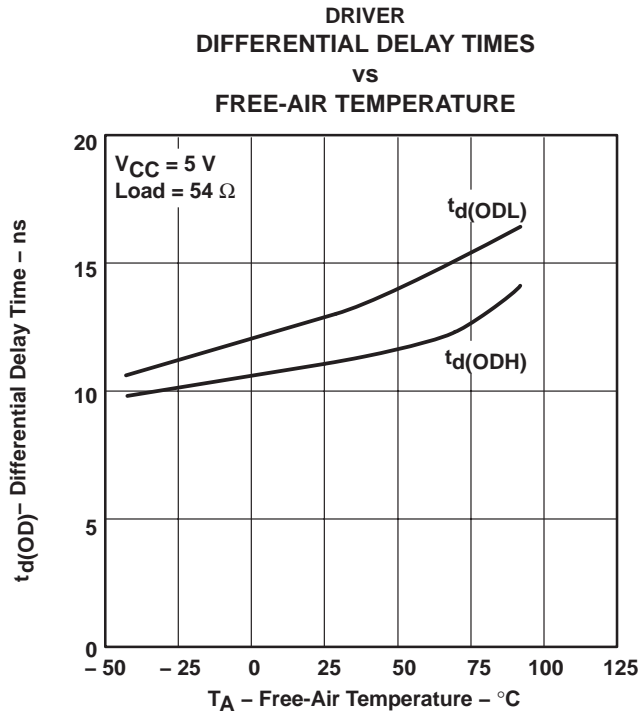


Figure 12

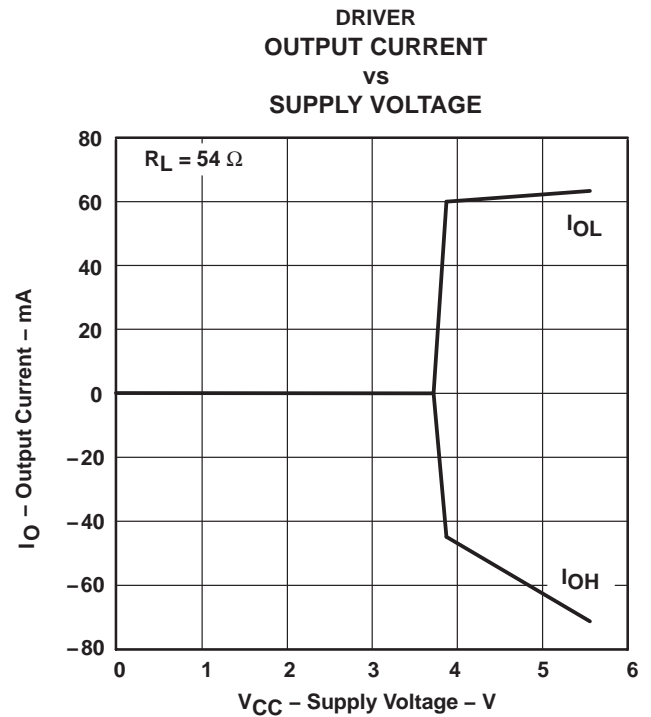


Figure 13

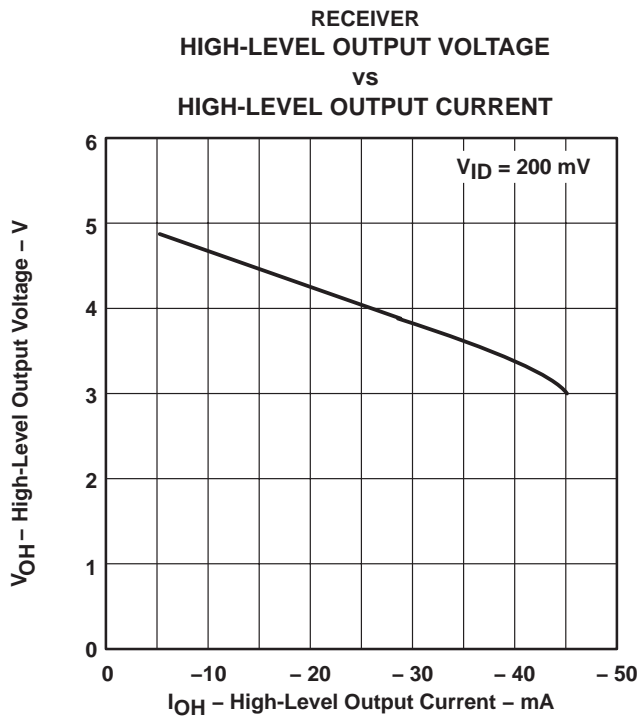


Figure 14

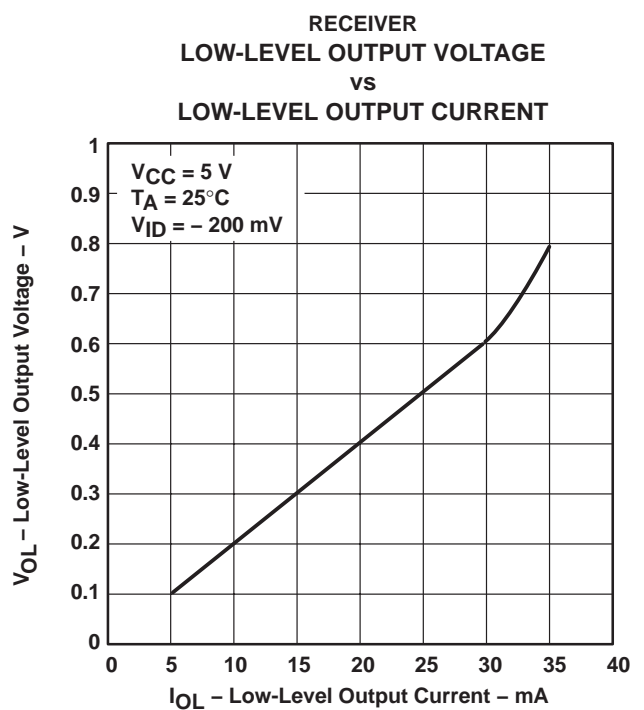


Figure 15

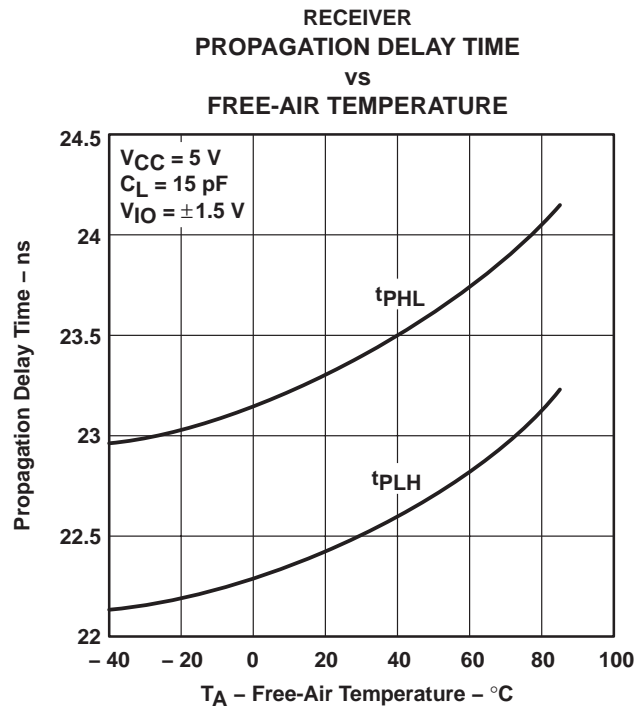
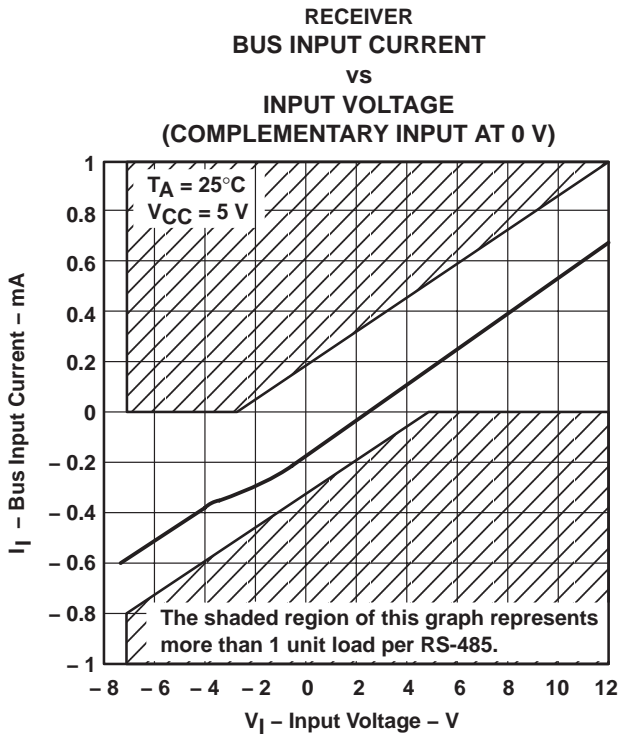
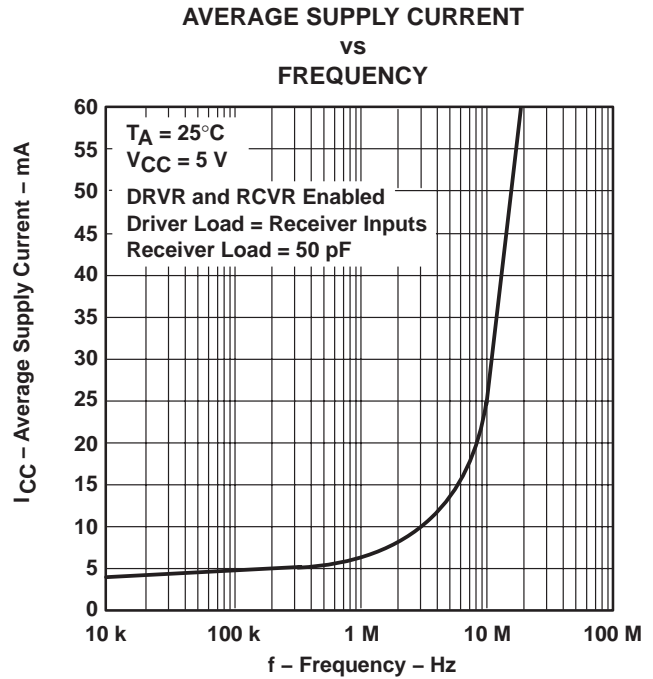
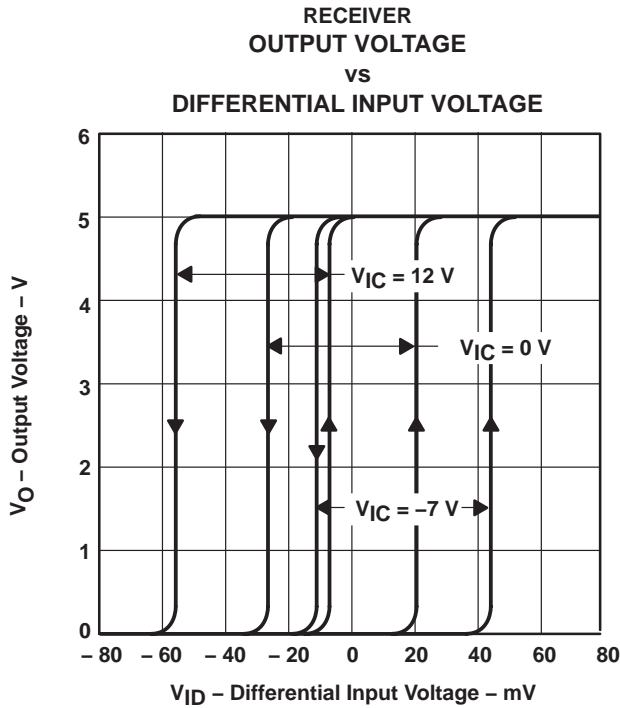


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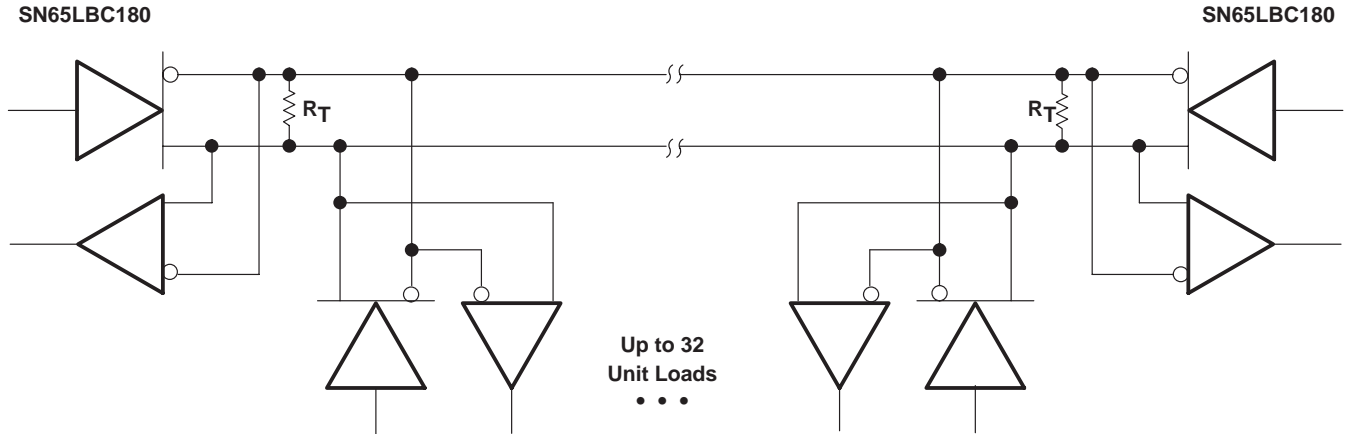
## LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIR

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### TYPICAL CHARACTERISTICS



APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible. One SN65LBC180 typically represents less than one unit load.

Figure 20. Typical Application Circuit

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC180IDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL180Q1	<a href="#">Samples</a>
SN65LBC180IDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LBC180IQ1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN65LBC180-Q1 :**

- Catalog: [SN65LBC180](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC180IDRG4Q1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC180IDRG4Q1	SOIC	D	14	2500	350.0	350.0	43.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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