

## N- and P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
N-Channel	40	0.0355 at V <sub>GS</sub> = 10 V	6.8	5.3
		0.0425 at V <sub>GS</sub> = 4.5 V	6.2	
P-Channel	- 40	0.045 at V <sub>GS</sub> = - 10 V	- 5.8	11.8
		0.062 at V <sub>GS</sub> = - 4.5 V	- 5.0	

### FEATURES

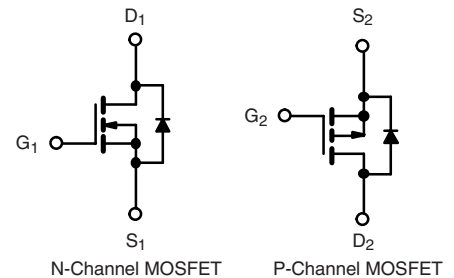
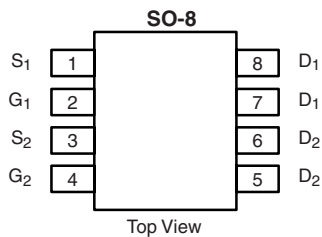
- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested



**RoHS**  
COMPLIANT

### APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge Converter



Ordering Information: Si4599DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V <sub>DS</sub>	40	- 40	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	6.8	- 5.8	A
		T <sub>C</sub> = 70 °C	5.4	- 4.7	
		T <sub>A</sub> = 25 °C	5.6 <sup>b, c</sup>	- 4.7 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	4.4 <sup>b, c</sup>	- 3.7 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	20	- 20		
Source-Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	2.5	- 2.5	
		T <sub>A</sub> = 25 °C	1.6 <sup>b, c</sup>	- 1.6 <sup>b, c</sup>	
Pulsed Source-Drain Current	I <sub>SM</sub>	20	- 20		
Single Pulse Avalanche Current	I <sub>AS</sub>	7	- 10	mJ	
Single Pulse Avalanche Energy	E <sub>AS</sub>	2.45	5		
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.0	3.1	W
		T <sub>C</sub> = 70 °C	1.9	2	
		T <sub>A</sub> = 25 °C	2.0 <sup>b, c</sup>	2.0 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	1.25 <sup>b, c</sup>	1.25 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	54	64	49	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	33	42	30	40	

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 120 °C/W.

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	40		V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-40			
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		44	mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-42		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-5.5		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		4.6		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.4		3.0	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1.2		-2.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			100	nA
			P-Ch			-100	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	$\mu\text{A}$
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	10			A
		$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-10			
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch		0.0295	0.0355	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	P-Ch		0.037	0.045	
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$	N-Ch		0.0355	0.0425	
		$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$	P-Ch		0.050	0.062	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 5\text{ A}$	N-Ch		22		S
		$V_{DS} = -15\text{ V}, I_D = -5\text{ A}$	P-Ch		14		
<b>Dynamic<sup>a</sup></b>							
Input Capacitance	$C_{iss}$	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		640		pF
			P-Ch		970		
Output Capacitance	$C_{oss}$	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		73		
			P-Ch		120		
Reverse Transfer Capacitance	$C_{rss}$		N-Ch		41		
			P-Ch		95		
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch		11.7	20	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	P-Ch		25	38	
		N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	N-Ch		5.3	9	
			P-Ch		11.8	18	
Gate-Source Charge	$Q_{gs}$	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	N-Ch		1.9		
			P-Ch		3.0		
Gate-Drain Charge	$Q_{gd}$		N-Ch		1.7		
			P-Ch		5.2		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	N-Ch	0.5	2.2	4.5	$\Omega$
			P-Ch	1.0	5.5	11	



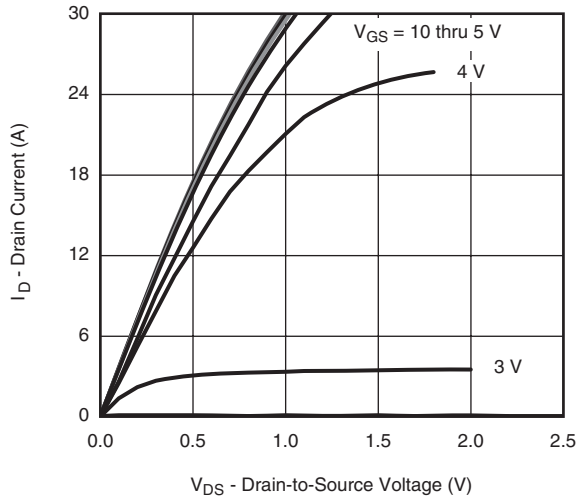
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit		
<b>Dynamic<sup>a</sup></b>								
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$ , $R_L = 4\ \Omega$ $I_D \cong 5\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		7	14	ns	
			P-Ch		7	14		
Rise Time	$t_r$		N-Ch		10	20		
			P-Ch		12	24		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$ , $R_L = 4\ \Omega$ $I_D \cong -5\text{ A}$ , $V_{GEN} = -10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		15	30		
			P-Ch		30	60		
Fall Time	$t_f$		N-Ch		9	18		
			P-Ch		9	18		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$ , $R_L = 4\ \Omega$ $I_D \cong 5\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		16	30		
			P-Ch		44	80		
Rise Time	$t_r$		N-Ch		17	30		
			P-Ch		33	50		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$ , $R_L = 4\ \Omega$ $I_D \cong -5\text{ A}$ , $V_{GEN} = -4.5\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		16	30		
			P-Ch		28	60		
Fall Time	$t_f$		N-Ch		10	20		
			P-Ch		13	25		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			2.5	A	
			P-Ch			-2.5		
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		N-Ch			20		
			P-Ch			-20		
Body Diode Voltage	$V_{SD}$	$I_S = 1.6\text{ A}$	N-Ch		0.78	1.2	V	
		$I_S = -1.6\text{ A}$	P-Ch		-0.76	-1.2		
Body Diode Reverse Recovery Time	$t_{rr}$	N-Channel $I_F = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		19	30	ns	
			P-Ch		26	50		
Body Diode Reverse Recovery Charge	$Q_{rr}$		P-Channel $I_F = -2\text{ A}$ , $di/dt = -100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		14	25	nC
				P-Ch		18.5	35	
Reverse Recovery Fall Time	$t_a$		N-Ch		13		ns	
			P-Ch		12.5			
Reverse Recovery Rise Time	$t_b$		N-Ch		6			
			P-Ch		13.5			

Notes:

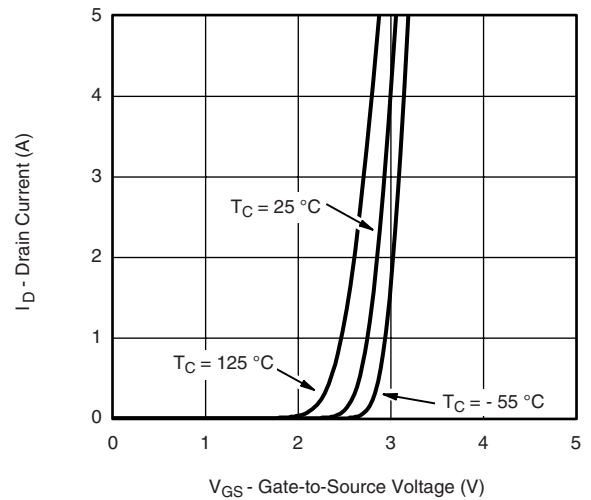
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

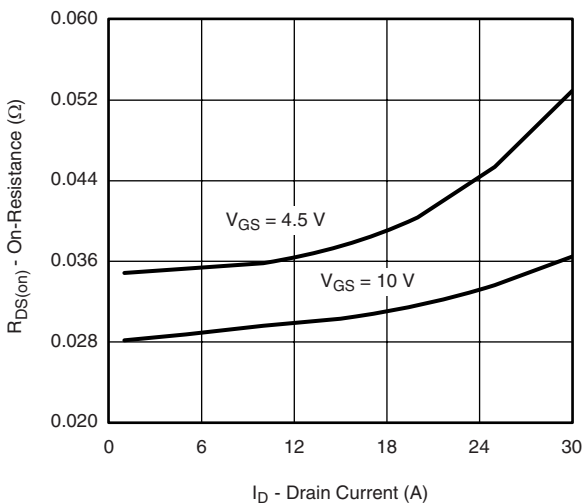
## N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



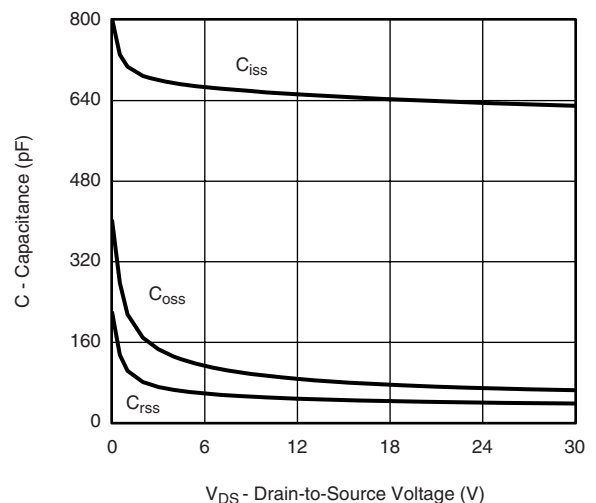
**Output Characteristics**



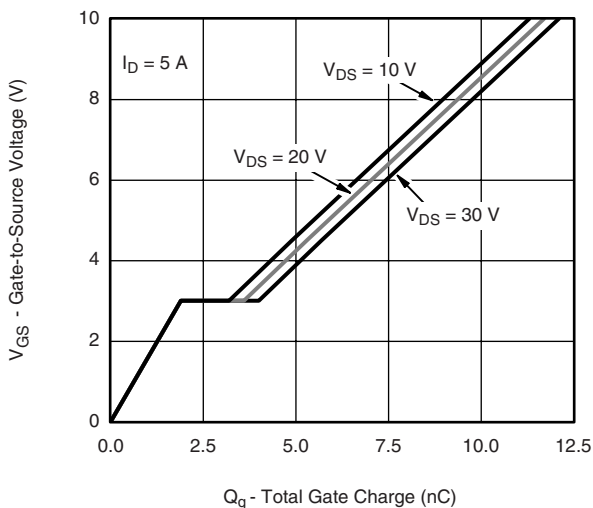
**Transfer Characteristics**



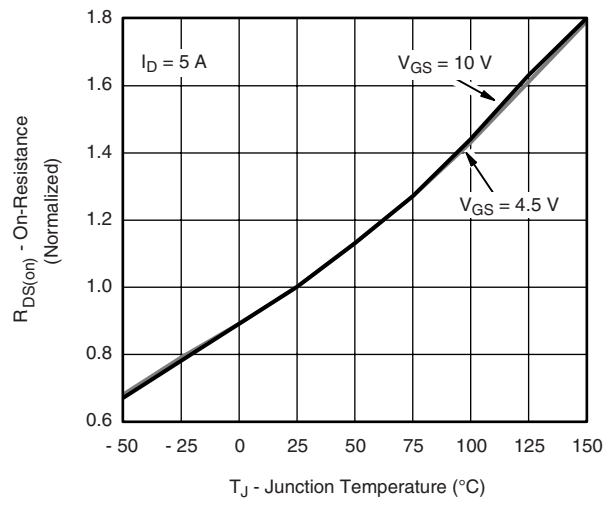
**On-Resistance vs. Drain Current**



**Capacitance**

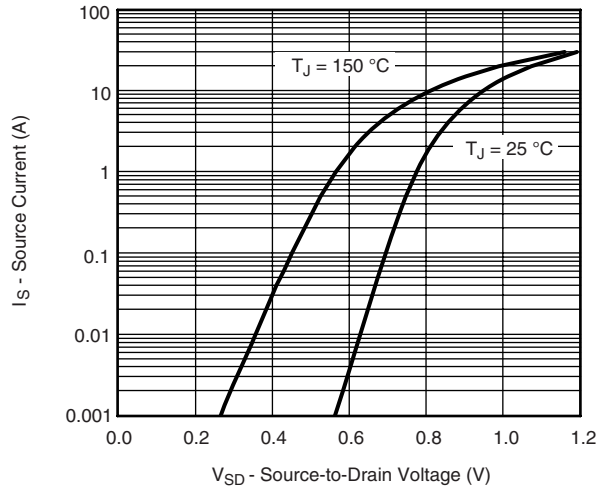


**Gate Charge**

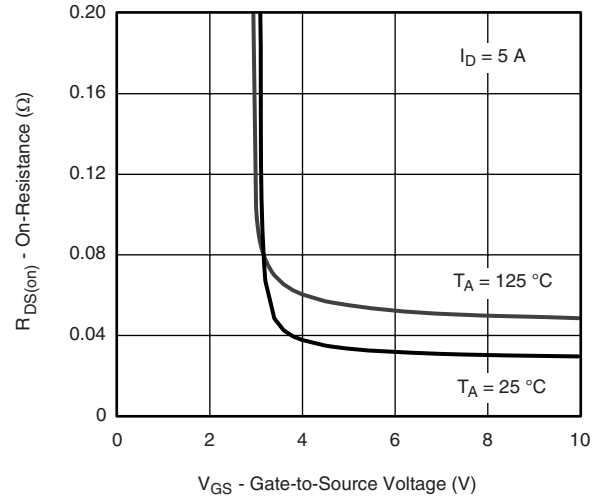


**On-Resistance vs. Junction Temperature**

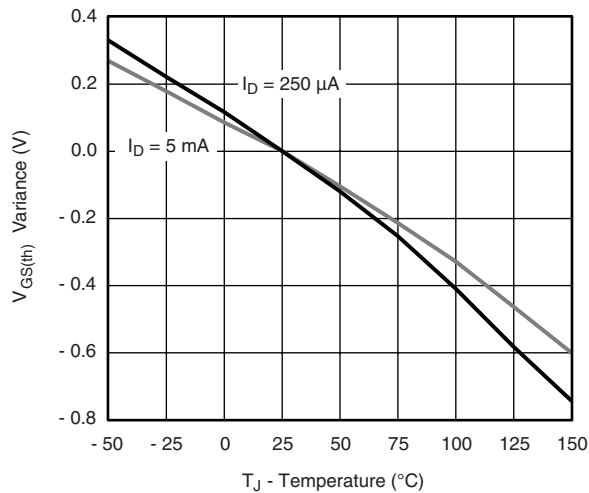
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



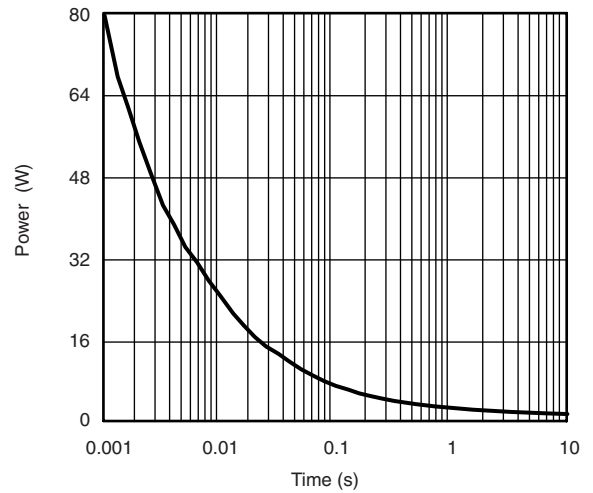
**Source-Drain Diode Forward Voltage**



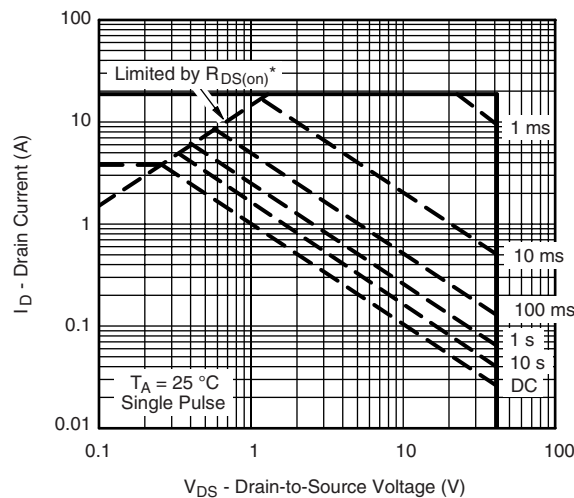
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



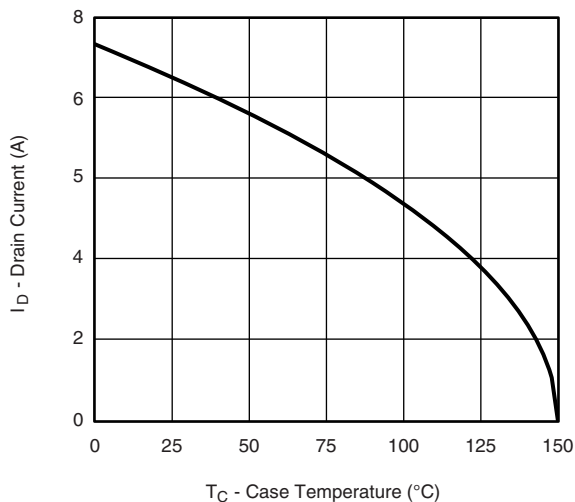
**Single Pulse Power, Junction-to-Ambient**



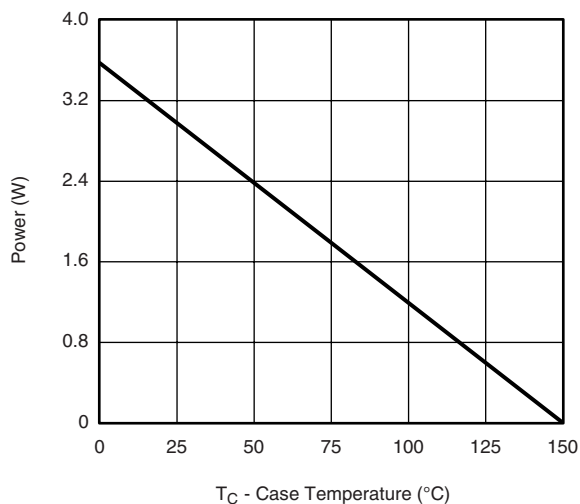
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

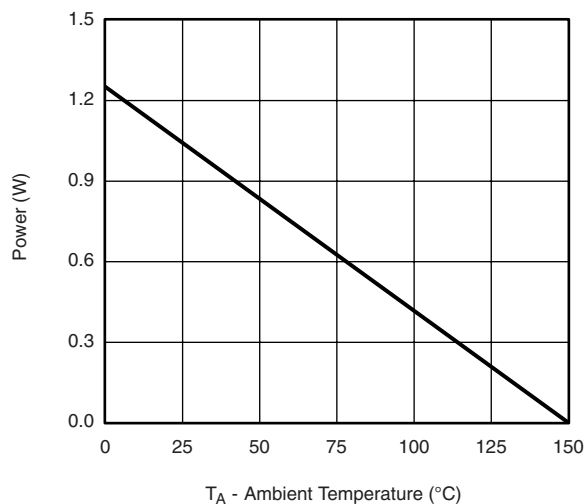
## N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



**Current Derating\***



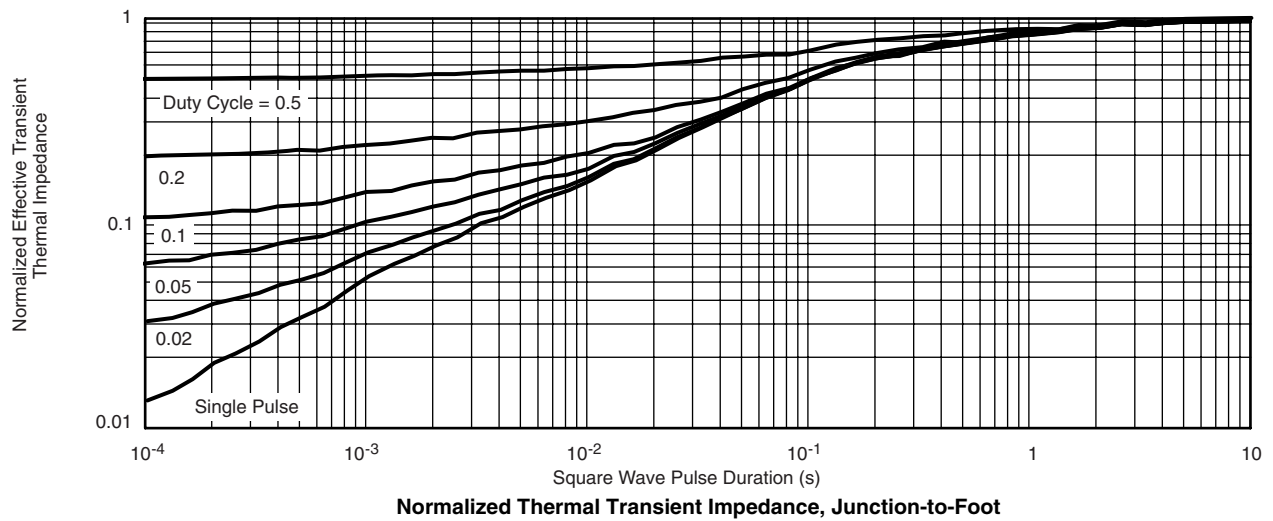
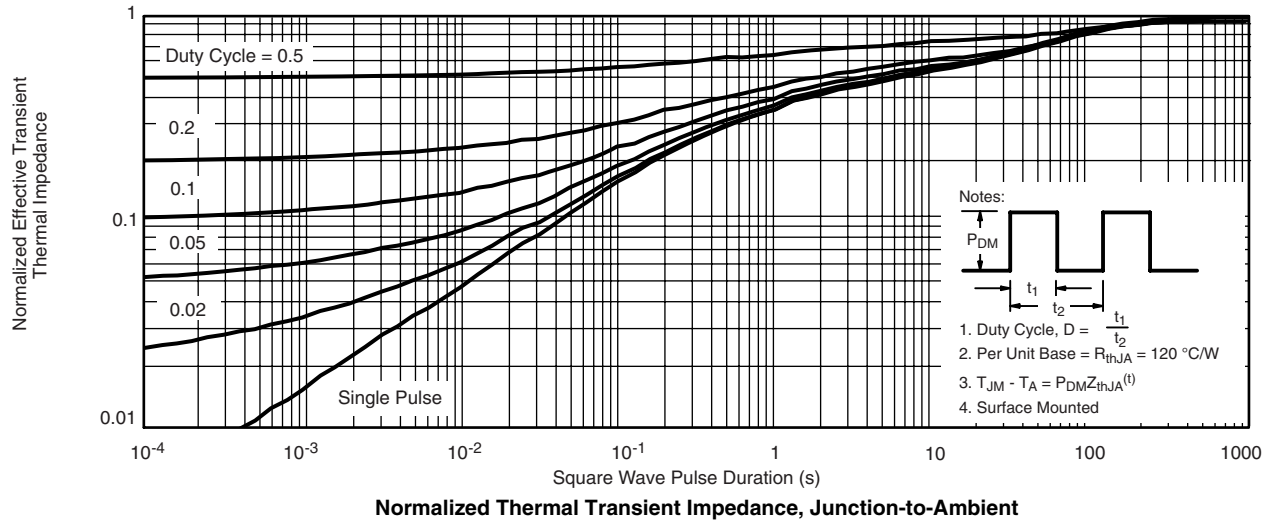
**Power Derating, Junction-to-Foot**



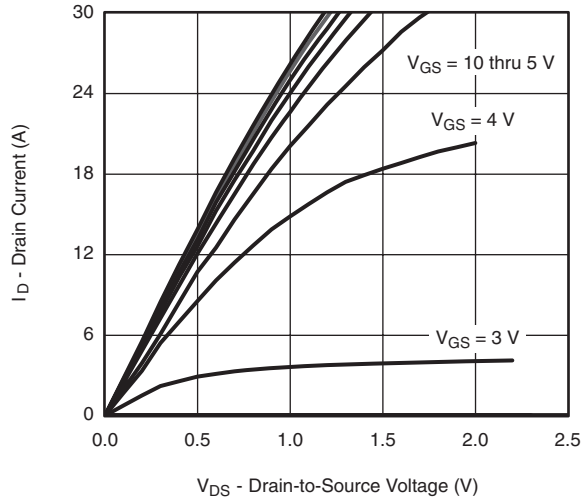
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

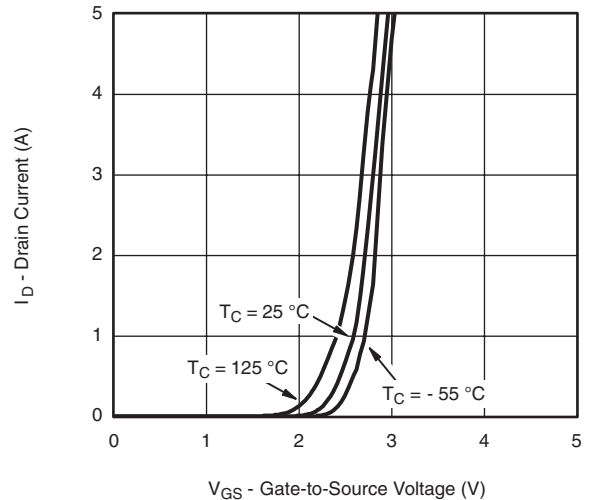
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



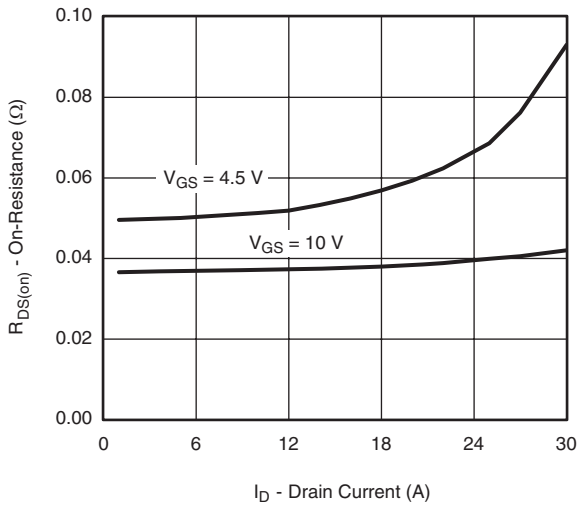
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



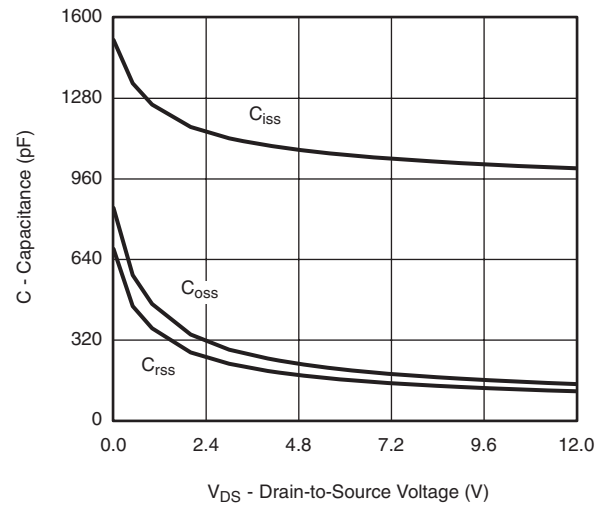
**Output Characteristics**



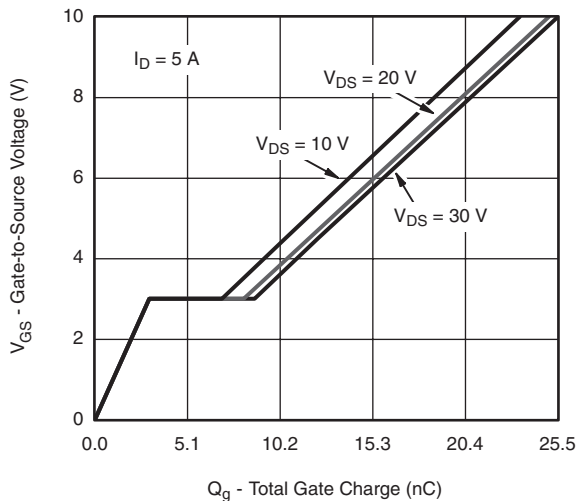
**Transfer Characteristics**



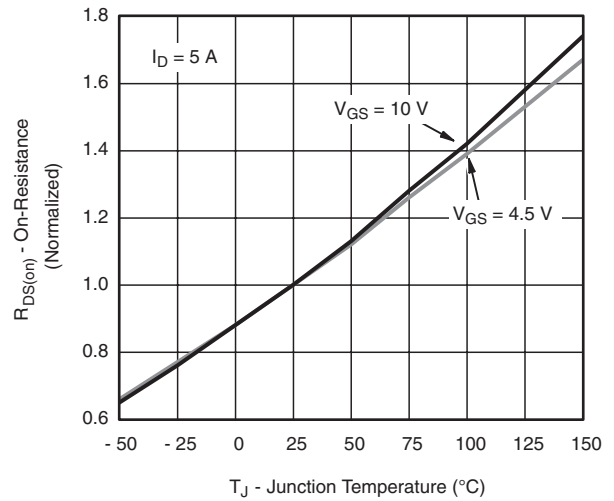
**On-Resistance vs. Drain Current**



**Capacitance**



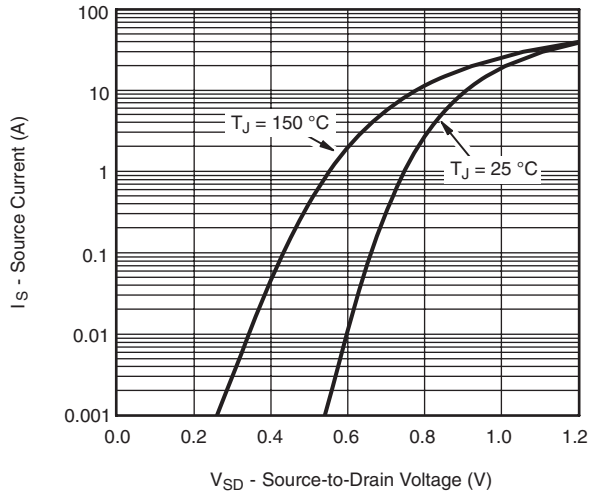
**Gate Charge**



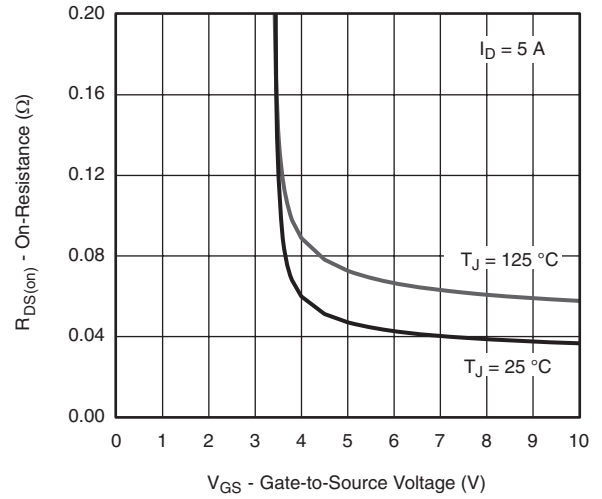
**On-Resistance vs. Junction Temperature**



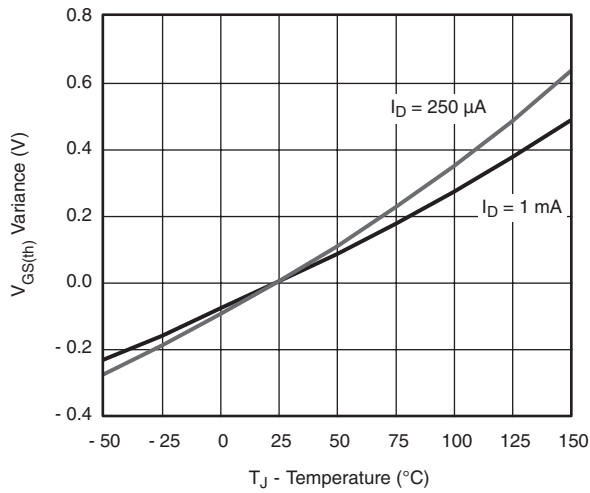
## P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



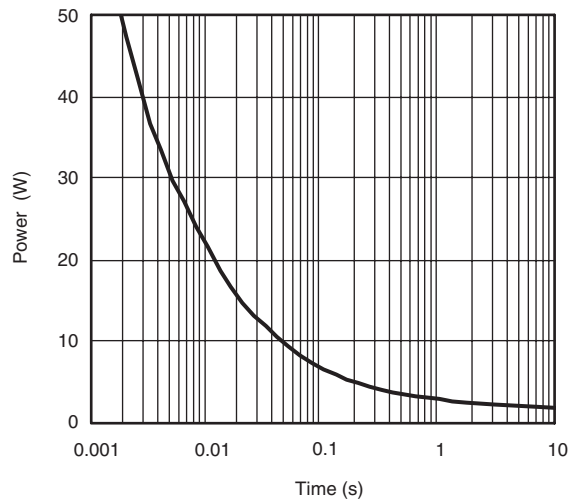
Source-Drain Diode Forward Voltage



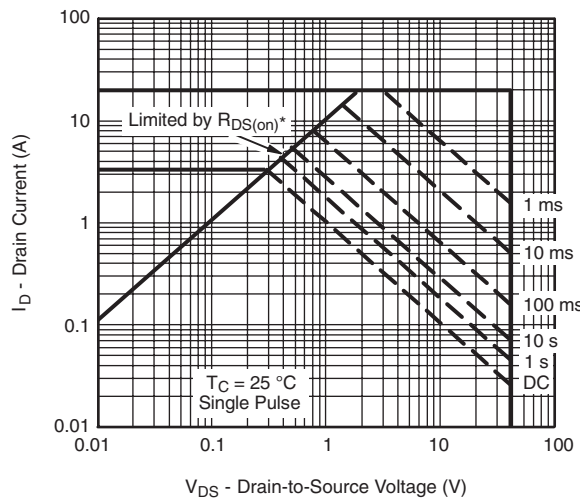
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



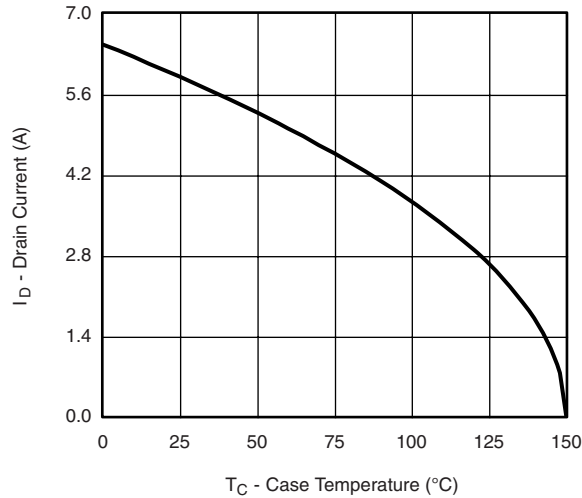
Single Pulse Power, Junction-to-Ambient



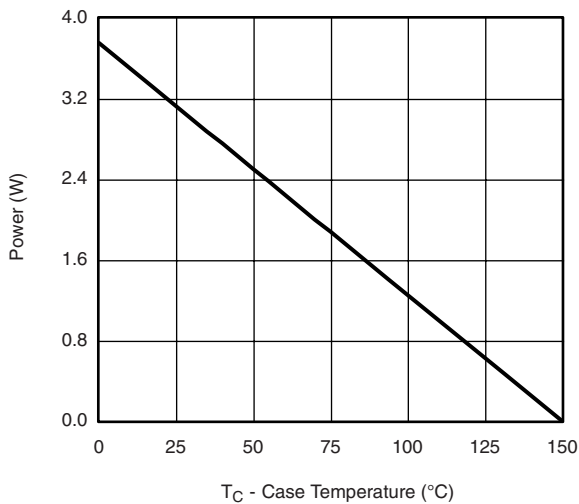
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

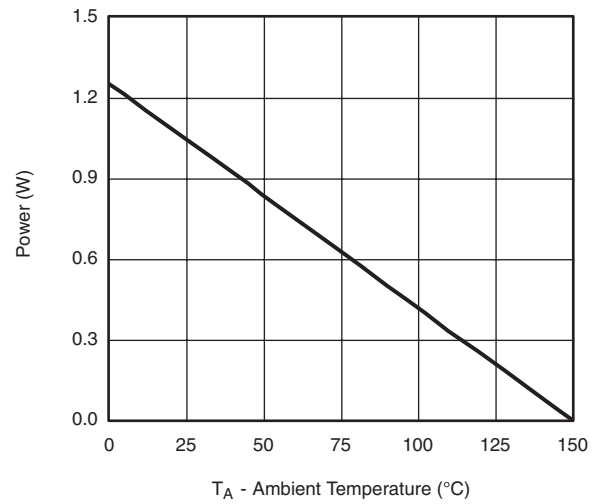
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\***



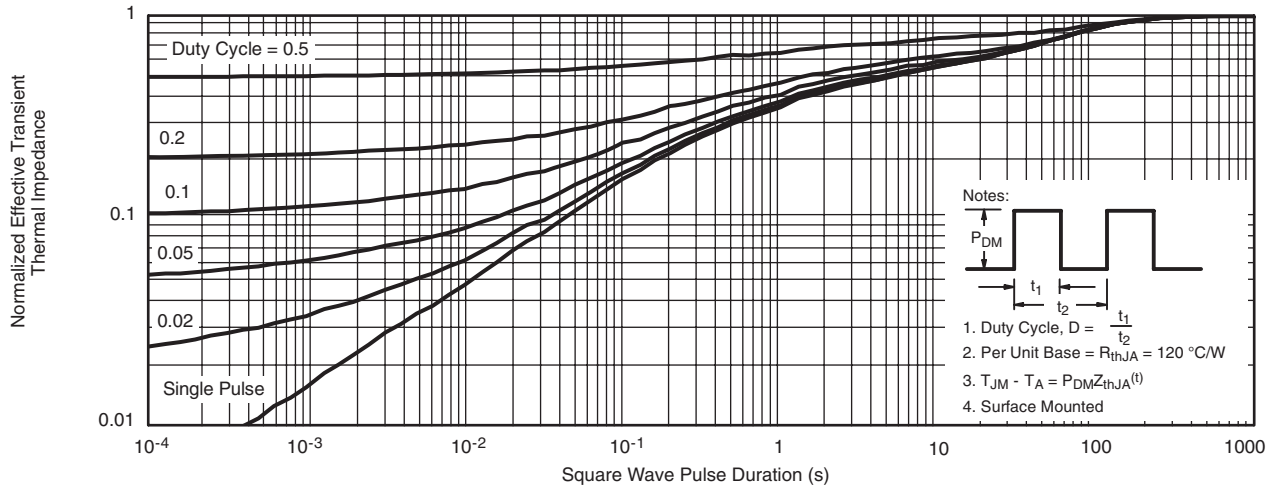
**Power Derating, Junction-to-Foot**



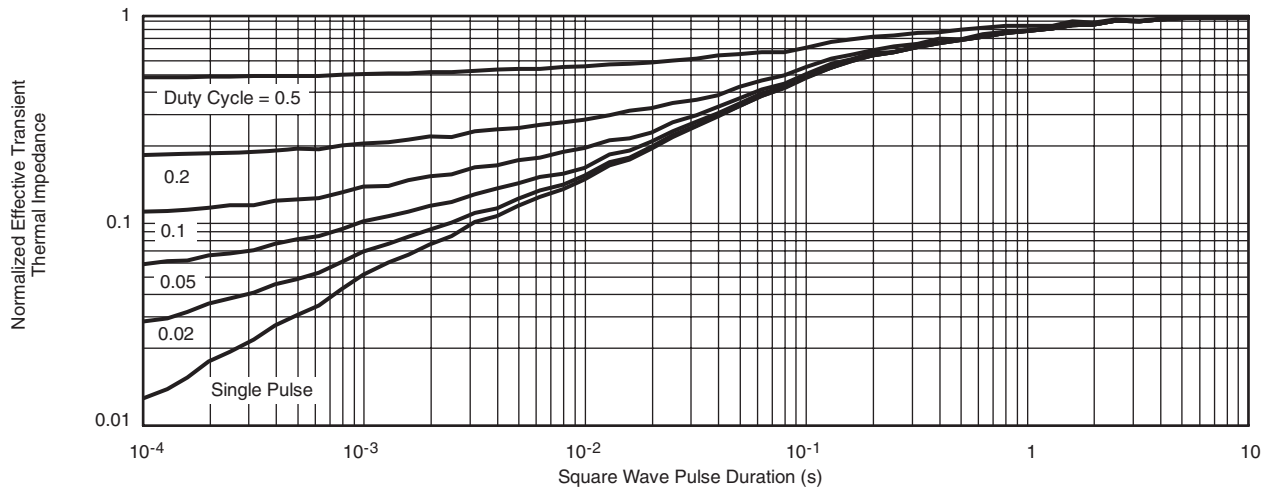
**Power Derating, Junction-to-Ambient**

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**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?68971>.

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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