

SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

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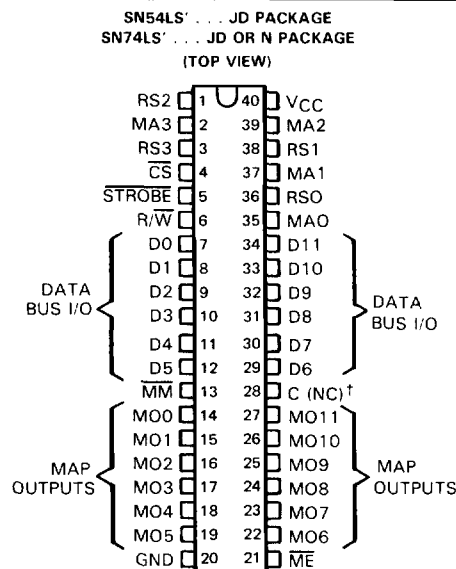
- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

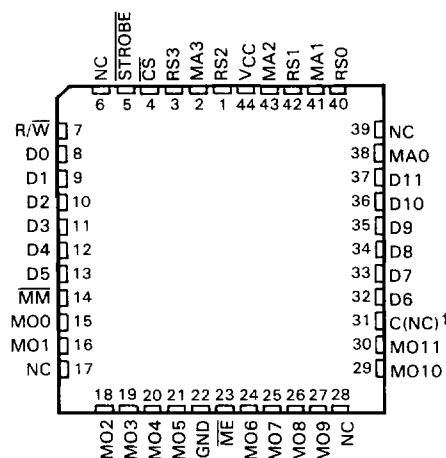
description

Each 'LS610 through 'LS613 memory-mapper integrated circuit contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. Each 'LS610 and 'LS611 also contains 12 latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see System Block Diagram) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus. This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).



SN54LS'... FK PACKAGE
SN74LS'... FN PACKAGE
(TOP VIEW)



† This pin has no internal connection on 'LS612 and 'LS613
NC—No internal connection

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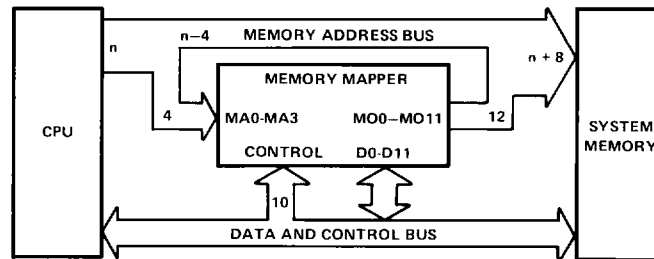
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INSTRUMENTS

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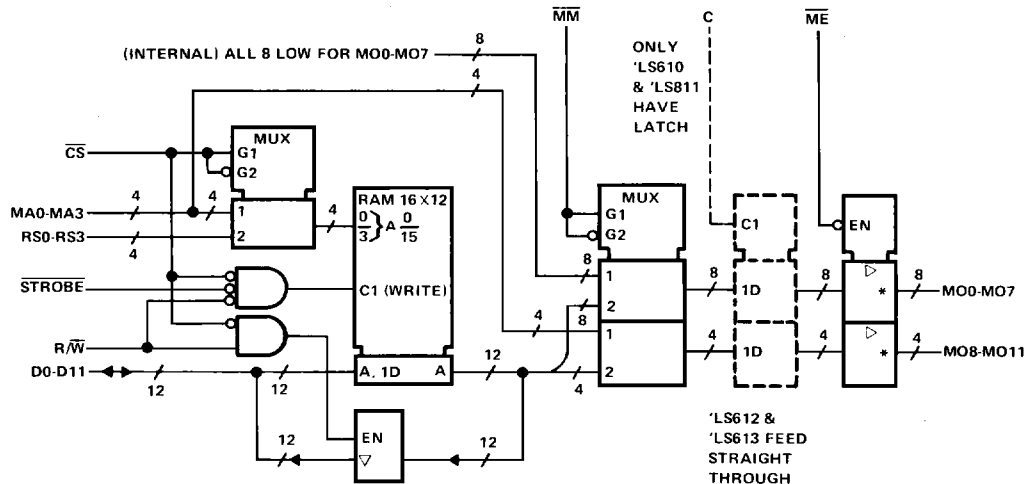
SYSTEM BLOCK DIAGRAM

These devices have four modes of operation: read, write, map, and pass. Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/W whenever chip select (\overline{CS}) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when \overline{CS} is high and MM (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When \overline{CS} and MM are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8-MO11, respectively, (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.

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logic diagram (positive logic)



*'LS610 and 'LS612 have 3-state (∇) map outputs.
'LS611 and 'LS613 have open collector (\square) map outputs.

**SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613
MEMORY MAPPERS**

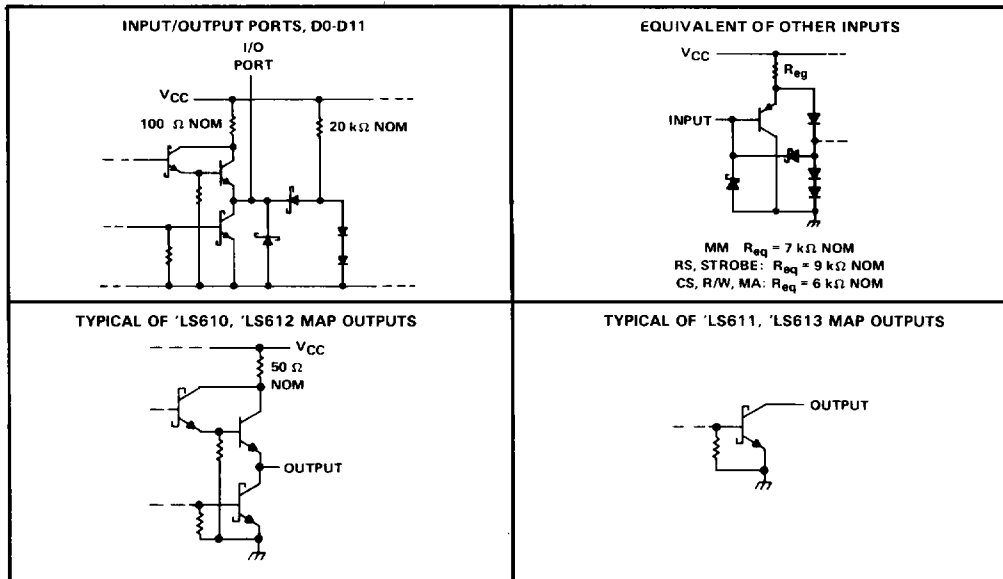
PIN		DESCRIPTION
NO.	NAME	
7-12 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when \overline{CS} is low. Mode controlled by R/W.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/W	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	STROBE	Strobe input used to enter data into the selected map register during I/O operations.
4	\overline{CS}	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode (\overline{MM} low and \overline{CS} high).
14-19, 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
13	\overline{MM}	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	\overline{ME}	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V _{CC} , GND	5 V power supply and network ground (substrate) pins.

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SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: Data Bus I/O	5.5 V
All other inputs	7 V
Operating free-air temperature range: SN54LS610 through SN54LS613	-55°C to 125°C
SN74LS610 through SN74LS613	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**SN54LS610, SN54LS612, SN74LS610, SN74LS612
MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS**

recommended operating conditions

			SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current	MO	-12			-15			mA
		D	-1			-2.6			
I _{OL}	Low-level output current	MO	12			24			mA
		D	4			8			
t _{AVCL}	Address setup time (AV before C low)	'LS610 only	See Figure 2	30		30			ns
t _{SLSH}	Duration of strobe input pulse			75		75			ns
t _{CSLSL}	\overline{CS} setup time (\overline{CS} low to strobe low)			20		20			ns
t _{WLSL}	R/ \overline{W} setup time (R/ \overline{W} low to strobe low)			20		20			ns
t _{RVSL}	RS setup time (RS valid to strobe low)			20		20			ns
t _{DVSH}	Data setup time (D0-D11 valid to strobe high)		See Figure 1	75		75			ns
t _{SHCSH}	\overline{CS} hold time (Strobe high to \overline{CS} high)			20		20			ns
t _{SHWH}	R/ \overline{W} hold time (Strobe high to R/ \overline{W} high)			20		20			ns
t _{SHRX}	RS hold time (Strobe high to RS invalid)			20		20			ns
t _{SHDX}	Data hold time (Strobe high to D0-D11 invalid)			20		20			ns
T _A	Operating free-air temperature			-55	125	0	70		°C

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LSI Devices

SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS610 SN54LS612		SN74LS610 SN74LS612		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5		V		
V _{OH}	MO D	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -3 mA	2.4		2.4	V	
			I _{OH} = MAX	2		2		
			I _{OH} = MAX	2.4		2.4		
V _{OL}	MO D	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA			0.35	0.5	
			I _{OL} = 4 mA	0.25	0.4	0.25	0.4	
			I _{OL} = 8 mA			0.35	0.5	
I _{OZH}		V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 2.7 V	20		20	μA		
I _{OZL}	MO	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 0.4 V	-20		-20	μA		
	D		-400		-400			
I _I	D	V _{CC} = MAX	V _I = 5.5 V	0.1		0.1	mA	
	All others		V _I = 7 V	0.1		0.1		
I _{IH}		V _{CC} = MAX, V _I = 2.7 V	20		20	μA		
I _{IL}		V _{CC} = MAX, V _I = 0.4 V	-0.4		-0.4	mA		
I _{OS} §	MO	V _{CC} = MAX	-40		-225	-40	-225	mA
	D		-30		-130	-30	-130	
I _{CC}		V _{CC} = MAX	Outputs high	112	180	112	180	mA
			Outputs low	112	180	112	180	
			Outputs disabled	150	230	180	230	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{CSDV}	Access (enable) time	C _S ↓	D0-11	R _L = 2 kΩ, See Figure 1, See Notes 2 and 3	28	50	26	50	ns	
t _{WHDV}	Access (enable) time	R/W↑	D0-11		20	35	20	35	ns	
t _{RVDV}	Access time	RS	D0-11		49	75	39	75	ns	
t _{WLDZ}	Disable time	R/W↓	D0-11		32	50	30	50	ns	
t _{CSDZ}	Disable time	C _S ↑	D0-11	42	65	38	65	ns		
t _{ELQV}	Access (enable) time	M _E ↓	MO0-11	R _L = 667 Ω, See Figure 2, See Notes 2 and 3	19	30	17	30	ns	
t _{CSHQV}	Access time	C _S ↑	MO0-11		56	85	48	85	ns	
t _{MLQV}	Access time	M _M ↓	MO0-11		25	40	22	40	ns	
t _{CHQV}	Access time	C↑	MO0-11		24	40			ns	
t _{AVQV1}	Access time (M _M low)	MA	MO0-11		46	70	39	70	ns	
t _{MHQV}	Access time	M _M ↑	MO0-11		24	40	22	40	ns	
t _{AVQV2}	Propagation time (M _M high)	MA	MO8-11		19	30	13	30	ns	
t _{EHQZ}	Disable time	M _E ↑	MO0-11		14	25	14	25	ns	

NOTES: 2. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

3. Load circuits and voltage waveforms are shown in Section 1.

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LSI Devices

**SN54LS611, SN54LS613, SN74LS611, SN74LS613
MEMORY MAPPERS WITH OPEN-COLLECTOR MAP OUTPUTS**

recommended operating conditions

		SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.7			V
V _{OH}	High-level output voltage	MO			5.5			V
I _{OH}	High-level output current	D			-1			mA
I _{OL}	Low-level output current	MO			12			24
		D			4			8
t _{AVCL}	Address setup time (AV before C low)	'LS611 only		See Figure 2	30		30	ns
t _{SLSH}	Duration of strobe input pulse				75		75	ns
t _{CSLSL}	\overline{CS} setup time (\overline{CS} low to strobe low)				20		20	ns
t _{WLSL}	R/ \overline{W} setup time (R/ \overline{W} low to strobe low)				20		20	ns
t _{RVSL}	RS setup time (RS valid to strobe low)				20		20	ns
t _{DVSH}	Data setup time (D0-D11 valid to strobe high)	See Figure 1		75		75	ns	
t _{SHCSH}	\overline{CS} hold time (Strobe high to \overline{CS} high)				20		20	ns
t _{SHWH}	R/ \overline{W} hold time (Strobe high to R/ \overline{W} high)				20		20	ns
t _{SHRX}	RS hold time (Strobe high to RS invalid)				20		20	ns
t _{SHDX}	Data hold time (Strobe high to D0-D11 invalid)				20		20	ns
T _A	Operating free-air temperature	-55		125	0		70	°C

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LSI Devices

SN54LS611, SN54LS613, SN74LS611, SN74LS613 MEMORY MAPPERS WITH OPEN-COLLECTOR MAP OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS611 SN54LS613		SN74LS611 SN74LS613		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V	
V _{OH}	D V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = MAX	2.4		2.4		V	
I _{OH}	MO V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V	0.1		0.1		mA	
V _{OL}	MO V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
		I _{OL} = 24 mA			0.35	0.5	
		I _{OL} = 4 mA	0.25	0.4	0.25	0.4	
I _{OL}	D V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 2.7 V	20		20		μA	
I _{OZL}	D V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V	-0.4		-0.4		mA	
I _I	D	V _I = 5.5 V		0.1		mA	
	All others	V _{CC} = MAX, V _I = 7 V		0.1			
I _{IH}	V _{CC} = MAX, V _I = 2.7 V	20		20		μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	-0.4		-0.4		mA	
I _{OS} §	D V _{CC} = MAX	-30	-130	-30	-130	mA	
I _{CC}	V _{CC} = MAX	Outputs high	100	170	100	170	mA
		Outputs low	100	170	100	170	
		Outputs disabled	110	200	110	200	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS611		'LS613		UNIT	
				MIN	TYP	MAX	MIN		TYP
t _{CSLDV}	Access (enable) time	\overline{CS} ↓	D0-11	R _L = 2 kΩ, See Figure 1, See Notes 2 and 3	31	50	28	50	ns
t _{WHDV}	Access (enable) time	R/W↑	D0-11		23	35	21	35	ns
t _{RVDV}	Access time	RS	D0-11		51	75	47	75	ns
t _{WLDZ}	Disable time	R/W↓	D0-11		32	50	31	50	ns
t _{CSHDZ}	Disable time	\overline{CS} ↑	D0-11		41	65	40	65	ns
t _{ELQV}	Access (enable) time	\overline{ME} ↓	MO0-11		21	30	19	30	ns
t _{CSHQV}	Access time	\overline{CS} ↑	MO0-11	R _L = 667 Ω, See Figure 2, See Notes 2 and 3	57	90	53	90	ns
t _{MLOV}	Access time	MM↓	MO0-11		25	40	25	40	ns
t _{CHQV}	Access time	C↑	MO0-11		30	45			ns
t _{AVQV1}	Access time (MM low)	MA	MO0-11		47	70	44	70	ns
t _{MHQV}	Access time	MM↑	MO0-11		31	50	31	50	ns
t _{AVQV2}	Propagation time (MM high)	MA	MO8-11		21	30	20	30	ns
t _{EHQZ}	Disable time	ME↑	MO0-11	15	25	15	25	ns	

NOTES: 2. Access times are tested as t_{PLH} and t_{PHL} or t_{PHZ} or t_{PLZ}. Disable times are tested as t_{PHZ} and t_{PLZ}.

3. Load circuits and voltage waveforms are shown in Section 1.

SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

explanation of letter symbols

This data sheet uses a new type of letter symbol based on JEDEC Standard 100 to describe time intervals. The format is:

t_{AB-CD}

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

- H = high or transition to high
- L = low or transition to low
- V = a valid steady-state level
- X = unknown, changing, or "don't care" level
- Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C SUBSCRIPT	SIGNAL NAME	A AND C SUBSCRIPT
C	C	ME	E
\overline{CS}	CS	MM	M
DO-11	D	R/W	W
MA0-MA3	A	RS0-RS3	R
MO0-MO11	Q	STROBE	S

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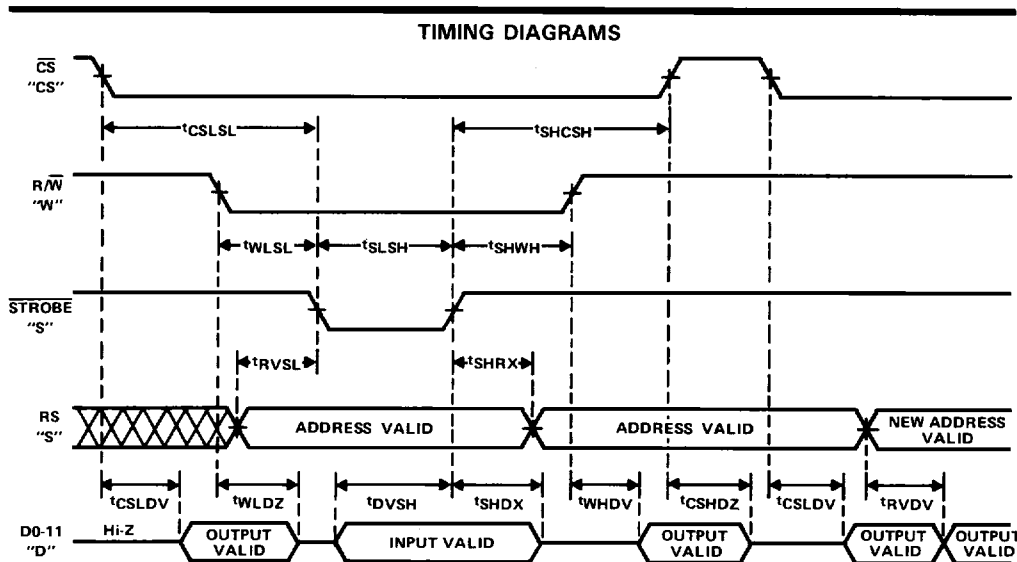


FIGURE 1. WRITE AND READ MODES

SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613
MEMORY MAPPERS

TIMING DIAGRAMS

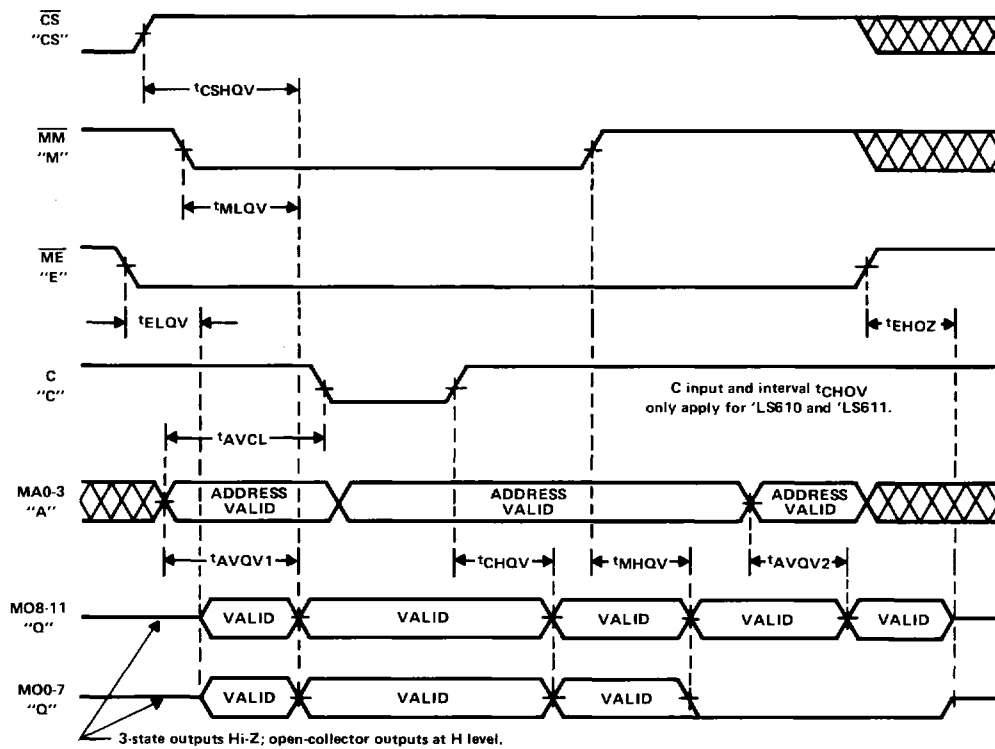


FIGURE 2. MAP AND PASS MODES

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