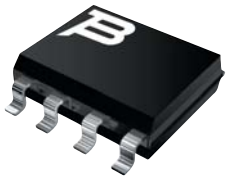
BOURNS®

Product Change Notification

TISP® THYRISTOR SURGE PROTECTORS

REVISED July 10, 2012



Model TISP9110LDMR-S
Die and Package Materials

Description of Changes

This Product Change Notification describes changes to the die and package materials in Bourns® Model TISP9110LDMR-S 8-Lead SOIC (210 mil) package to improve the part's robustness and optimize the manufacturing process.

The metallization of one of the dies has been changed from Al to NiAu to improve its robustness under 85 °C/ 85 % RH reliability testing. Nickel/Gold is currently present on the backside of the die as a contact metallization. One mask layer in the metal deposition flow process is changed to achieve the desired metal strap NiAu coating.

Furthermore, the existing 2 mil gold wire is changed to 2 mil copper wire. All bond wires will be configured with a ball bond to the die and a stitch (wedge) bond to the leadframe finger. Chip to chip bond wires are eliminated by modifying the leadframe design to accept extra bond wires connected directly to the Tip and Ring pin outs. The use of Copper bond wire is a proven technology, and is the technology of choice for Bourns® TISP6 products manufactured in 8-Lead SOIC (150 mil) packages since 4Q09. Using Cu bond wires in the TISP9110LDMR-S will limit future exposure to rising gold prices and shortages.

To accommodate the use of Cu wires, the leadframe internal die pad and bond finger layouts are adjusted to increase the available wire bonding area on the Tip and Ring pins. All external pin outs remain the same with no change to the product data sheet specifications.

Bourns® Model TISP9110LDMR-S devices utilize two similar die to realize the protection functionality. Each die has been reconfigured to provide the same performance in a smaller total area, in order to allow space to accommodate the change in leadframe and conversion to copper wire bonding. Each die consists of a gate buffer transistor with a pair of SCRs triggered to the on-state by an overvoltage appearing on the Tip or Ring. The buffer transistor layout remains in the same area but the voltage breakdown capability has been increased by incorporating additional diffused features by a mask change. The main SCR areas are unchanged but additional diffused features increase the voltage breakdown capability of the SCR. Consequently, the surge ratings of the die will remain unchanged at a level significantly higher than the product data sheet specification, while the voltage blocking robustness of the product is increased.

There are no changes to the Bourns® Model TISP9110LDMR-S data sheet ratings or electrical characteristics and the improvements in robustness are achieved by modification to mask layers only. The wafer fab process flow and process settings are not changed for this product.

Qualification Requirements

Assessment of the appropriate qualification stress test for each of the changes is made in agreement with Bourns Major Change Control Specification 14-0503. The identified change categories requiring qualification are:

Design	Design Change
Die	Die Size
Die	Spacing/Isolation
Leadframe	Critical Dimensions
Bonding	Bond Wire Material

Qualification Plan

Planned Reliability Qualification tests are listed in Table 1.
Electrical characterization tests for validation of data sheet ratings are listed in Table 2.

Qualification Timing

Qualification testing is expected to be completed at end of September 2012.

Product Labeling

The product marking and labels are unchanged.

Identification of the Changed Product

Bourns maintains traceability back to source wafer lots and assembly sites for all TISP® products.

Impact on Form, Fit, Function and Reliability

Product ratings and electrical characteristics are unaffected by the change. There is no impact on form, fit, function or reliability.

Samples

Evaluation samples are available from August 2012 onward.

Implementation Date

First date code using above changes: 1246
Deliveries of such products may occur from January 2013 onward.

If you have any questions, please contact our customer service teams in your region.

Table 1: Qualification Test Plan

Item No.	Stress Test	Reference	Conditions	Duration	Read Points	No. of Lots	Sample Size	LTPD	Accept/ Reject
1	Preconditioning	JESD22A-113	260 °C	3x		Prior to Tests 2,3 & 4			
2	High Temperature Reverse Bias	JESD22-A108	T_j>125 °C, V_r>80 %	1000 hrs.	168, 500 hrs.	3	76	3	0/1
3	Temperature Cycle	JESD22-A104	-55 °C / +150 °C	1000 cs	100, 500, 700 cs	3	76	3	0/1
4	High Humidity High Temperature Reverse Bias	JESD22-A101	85 °C / 85 % RH, V_r>80 %	1000 hrs		3	32	7	0/1
5	ESD-IBM	JESD22-A114	25 °C			1	10		0/1
6	Die Shear Strength	MIL-STD-883, Method 2019.7				3	32	7	0/1
7	Bond Pull Strength	MIL-STD-883, Method 2011.7				3	32	7	0/1
8	Wire Bond Shear	JESD22-B116				3	32	7	0/1
9	Electrical Parameter Assessment	JESD86	Data Sheet			3	32	7	

Table 2: Product Data Sheet Validation Test Plan

Symbol	Data Sheet Rating/Parameter	Conditions	Data Sheet	No. of Lots	Sample Size
I_{PPSM}	Non-repetitive peak impulse current	10/1000 µs	30 A	3	32
		5/310 µs	45 A	3	32
		2/10 µs	100 A	3	32
I_{TSM}	Non-repetitive peak on-state current	0.2 s, 50 Hz	9 A	3	32
		1 s, 50 Hz	5 A	3	32
		900 S, 50 Hz	1.7 A	3	32
I_D	Off-state current	V_D = -120 V, $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V, T_A = 85 °C	-50 µA Max.	3	32
		V_D = -120 V, $V_{G2(Line)}$ = 0, V_{G1} ≥ +5 V, T_A = 85 °C	+50 µA Max.	3	32
$V_{G1L(BO)}$	Gate - Line impulse breakover voltage	V_{G1} = -100 V, I_T = -100 A 2/10 µs	-15 V Max.	3	32
		V_{G1} = -100 V, I_T = -30 A 10/1000 µs	-11 V Max.	3	32
$V_{G2L(BO)}$	Gate - Line impulse breakover voltage	V_{G2} = +100 V, I_T = +100 A 2/10 µs	15 V Max.	3	32
		V_{G2} = +100 V, I_T = +30 A 10/1000 µs	11 V Max.	3	32
C_O	Capacitance	f = 1 MHz, V_D = -3 V, G1 & G2 open circuit	32 pF Typ.	1	32