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August 2018

FDMS8622

N-Channel Shielded Gate PowerTrench® MOSFET
100 V, 16.5 A, 56 mΩ

Features

- Shielded Gate MOSFET Technology

- Max $r_{DS(on)}$ = 56 mΩ at V_{GS} = 10 V, I_D = 4.8 A

- Max $r_{DS(on)}$ = 88 mΩ at V_{GS} = 6 V, I_D = 3.9 A

- High performance trench technology for extremely low $r_{DS(on)}$

- High power and current handling capability in a widely used surface mount package

- 100% UIL Tested

- Termination is Lead-free and RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- POE Protection Switch

- DC-DC Switch
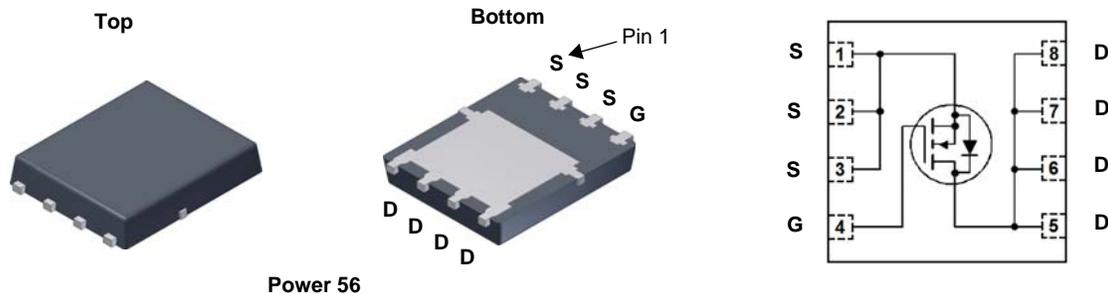
Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		16.5	A
	-Continuous	T_A = 25 °C	(Note 1a)	4.8	
	-Pulsed			30	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	12	mJ
P_D	Power Dissipation	T_C = 25 °C		31	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		(Note 1)	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8622	FDMS8622	Power56	13 ''	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		69		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		-8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.8 A		45	56	mΩ
		V_{GS} = 6 V, I_D = 3.9 A		62	88	
		V_{GS} = 10 V, I_D = 4.8 A, T_J = 125 °C		78	97	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 4.8 A		9		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		301	400	pF
C_{oss}	Output Capacitance			70	95	pF
C_{rss}	Reverse Transfer Capacitance			3.6	5	pF
R_g	Gate Resistance			1.0		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 4.8 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		5.7	11	ns
t_r	Rise Time			1.7	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10.2	18	ns
t_f	Fall Time			2.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V		5	7	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V V_{DD} = 50 V, I_D = 4.8 A		2.8	4	nC
Q_{gs}	Total Gate Charge			1.4	2.8	nC
Q_{gd}	Gate to Drain "Miller" Charge			1.3	2.6	nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 4.8 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 4.8 A, di/dt = 100 A/µs		38	60	ns
Q_{rr}	Reverse Recovery Charge			30	48	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
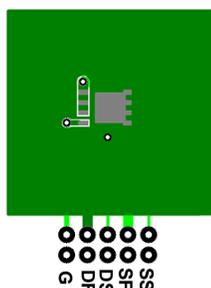
a) 50 °C/W when mounted on a 1 in² pad of 2 oz copper
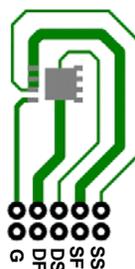
b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. Starting T_J = 25 °C; N-ch: L = 0.1 mH, I_{AS} = 16 A, V_{DD} = 90 V, V_{GS} = 10 V.

Typical Characteristics T_J = 25 °C unless otherwise noted
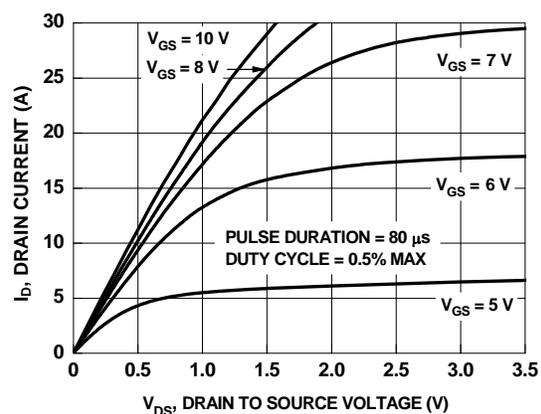
Figure 1. On Region Characteristics
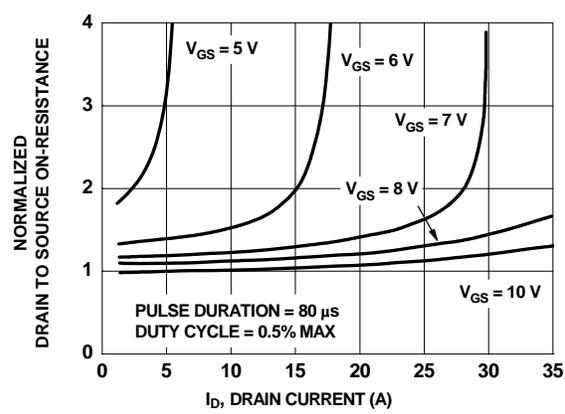
Figure 2. Normalized On-Resistance
vs Drain Current and Gate Voltage
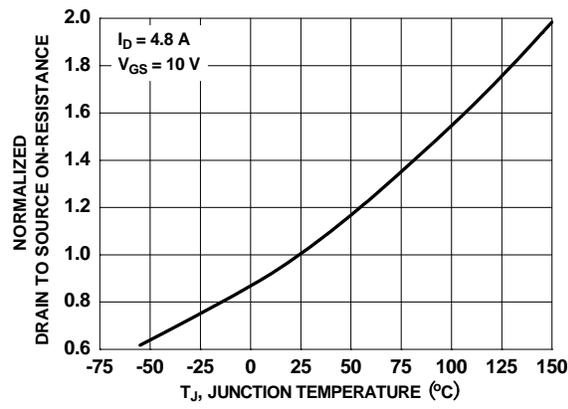
Figure 3. Normalized On Resistance
vs Junction Temperature
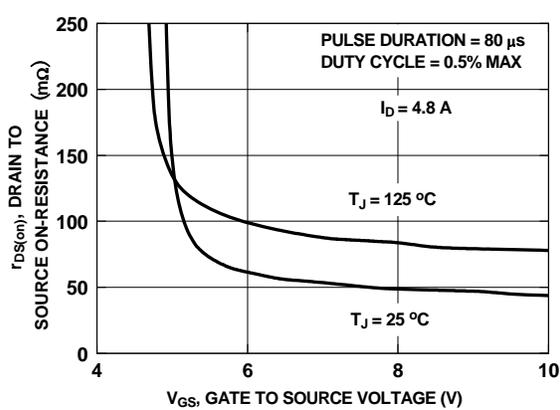
Figure 4. On-Resistance vs Gate to
Source Voltage
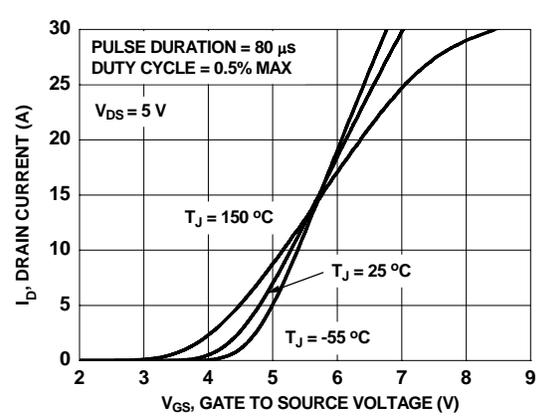
Figure 5. Transfer Characteristics
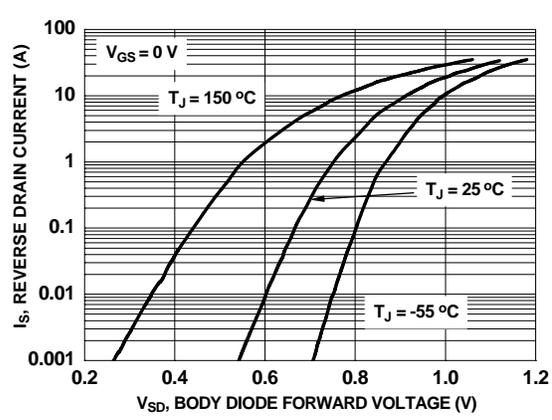
Figure 6. Source to Drain Diode
Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted
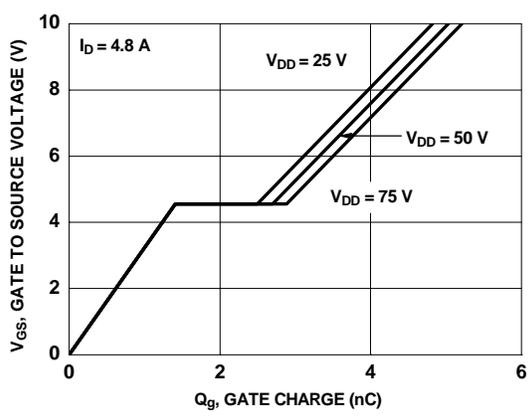
Figure 7. Gate Charge Characteristics
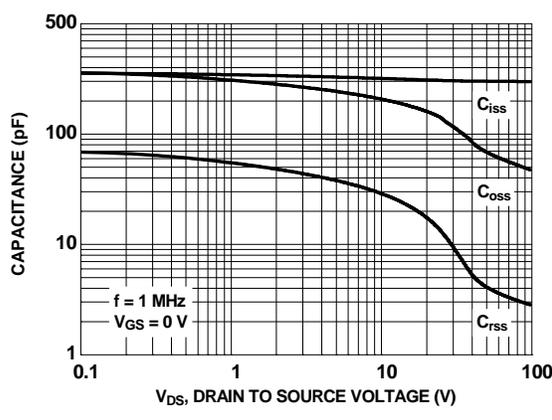
Figure 8. Capacitance vs Drain to Source Voltage
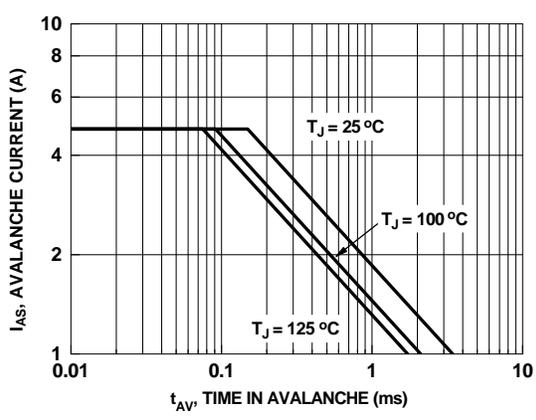
Figure 9. Unclamped Inductive Switching Capability
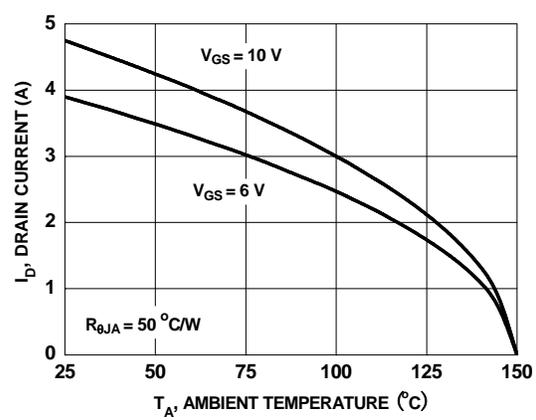
Figure 10. Maximum Continuous Drain Current vs Ambient Temperature
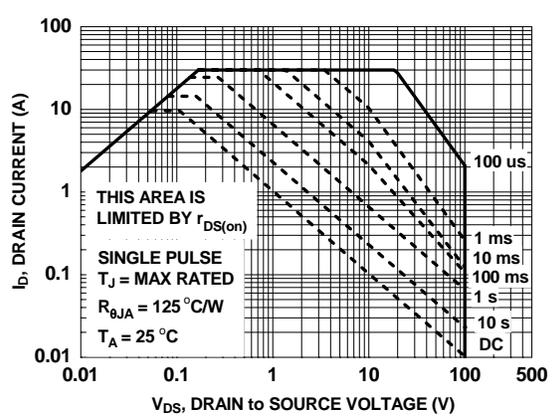
Figure 11. Forward Bias Safe Operating Area
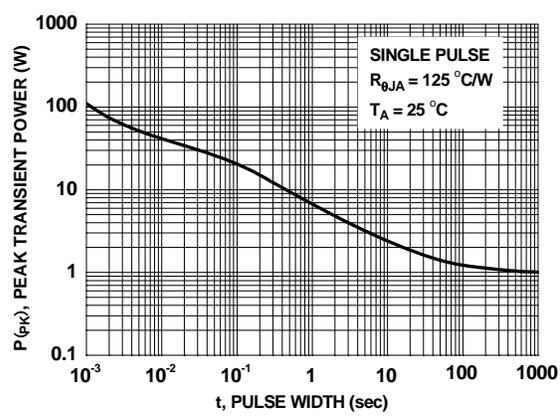
Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted
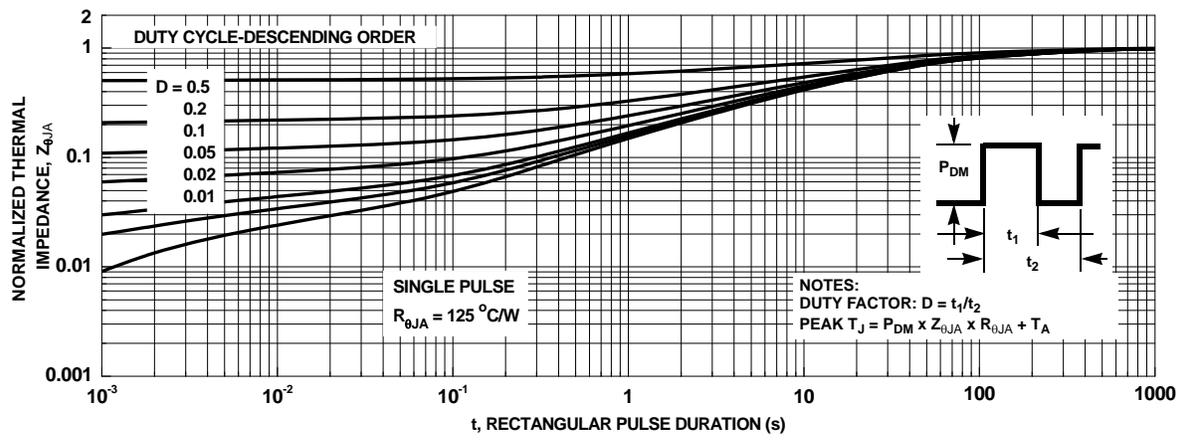
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout

TOP VIEW

5.20 / 4.80

PKG ℄

6.25 / 5.90

PKG ℄

A

B

8 5

1 4

SEE DETAIL B

5.85 / 5.65

LAND PATTERN RECOMMENDATION

5.10

3.91

0.64

1.27

0.77

4.52

3.75

6.61

8 7 6 5

1 2 3 4

KEEP OUT AREA

1.27

1.27

3.81

0.61

SIDE VIEW

5.00 / 4.80

SEE DETAIL C

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE

// 0.10 C

8X

◠ 0.08 C

1.10 / 0.90

0.35 / 0.15

0.05 / 0.00

C

SEATING PLANE

DETAIL C
SCALE: 2:1

0.35 / 0.15

0.30 / 0.06

DETAIL B
SCALE: 2:1

BOTTOM VIEW

3.81

1.27

0.51 / 0.31 (8X)

(0.34)

⊕ 0.10 Ⓜ C A B

0.76 / 0.44

1 2 3 4

(0.52)

(0.50)

(3.40)

(0.30) (2X)

3.78 / 3.38

4.22 / 3.99

8 7 6 5

0.64 / 0.34

3.96 / 3.61

NOTES: UNLESS OTHERWISE SPECIFIED
A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F. DRAWING FILE NAME: PQFN08AREV8

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