

# 74ACT841

## 10-Bit Transparent Latch with 3-STATE Outputs

### General Description

The ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The ACT841 is a 10-bit transparent latch, a 10-bit version of the ACT373.

### Features

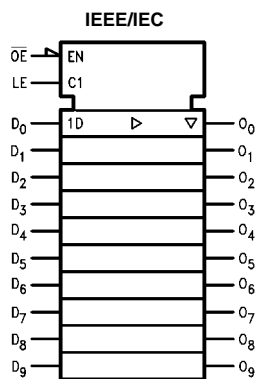
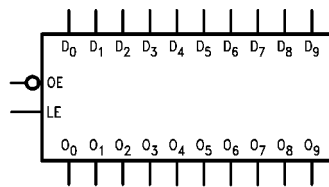
- ACT841 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Non-inverting 3-STATE outputs

### Ordering Code:

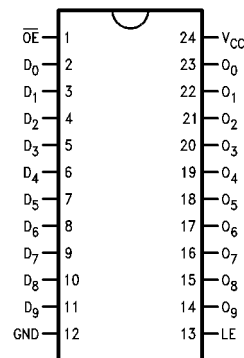
Order Number	Package Number	Package Description
74ACT841SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT841MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT841SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (SPC not available in Tape and Reel.)

### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>9</sub>	Data Inputs
O <sub>0</sub> -O <sub>9</sub>	3-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

FACT™ is a trademark of Fairchild Semiconductor Corporation.

## Functional Description

The ACT841 consists of ten D-type latches with 3-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

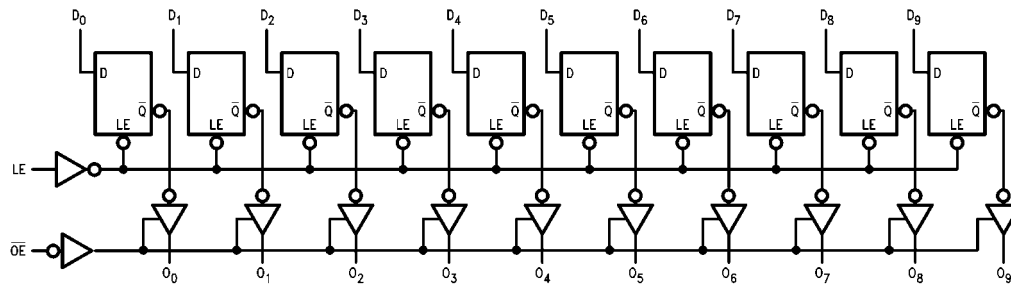
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

## Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings <sup>(Note 1)</sup>		Recommended Operating Conditions	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
DC Input Diode Current ( $I_{IK}$ )		Input Voltage ( $V_I$ )	0V to $V_{CC}$
$V_I = -0.5V$	-20 mA	Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_I = V_{CC} + 0.5V$	+20 mA	Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
DC Output Diode Current ( $I_{OK}$ )		$V_{IN}$ from 0.8V to 2.0V	
$V_O = -0.5V$	-20 mA	$V_{CC}$ @ 4.5V, 5.5V	
$V_O = V_{CC} + 0.5V$	+20 mA		
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$		
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA		
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA		
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C		
Junction Temperature ( $T_J$ )			
PDIP	140°C		

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

### DC Electrical Characteristics

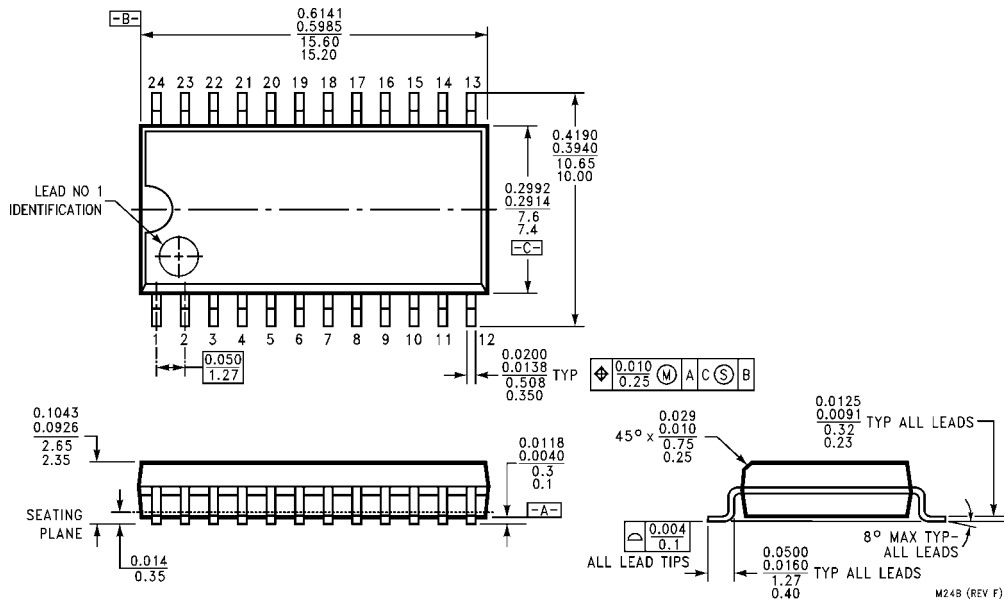
Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
$V_{IL}$	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
$V_{OH}$	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$
$V_{OL}$	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$
$I_{OZ}$	Maximum 3-STATE Leakage Current	5.5		$\pm 0.5$	$\pm 5.0$	$\mu A$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
$I_{CCT}$	Maximum $I_{CC}/Input$	5.5	0.6		1.5	$\mu A$	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min
$I_{CC}$	Maximum Quiescent Supply Current	5.5		8.0	80.0	$\mu A$	$V_{IN} = V_{CC}$ or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

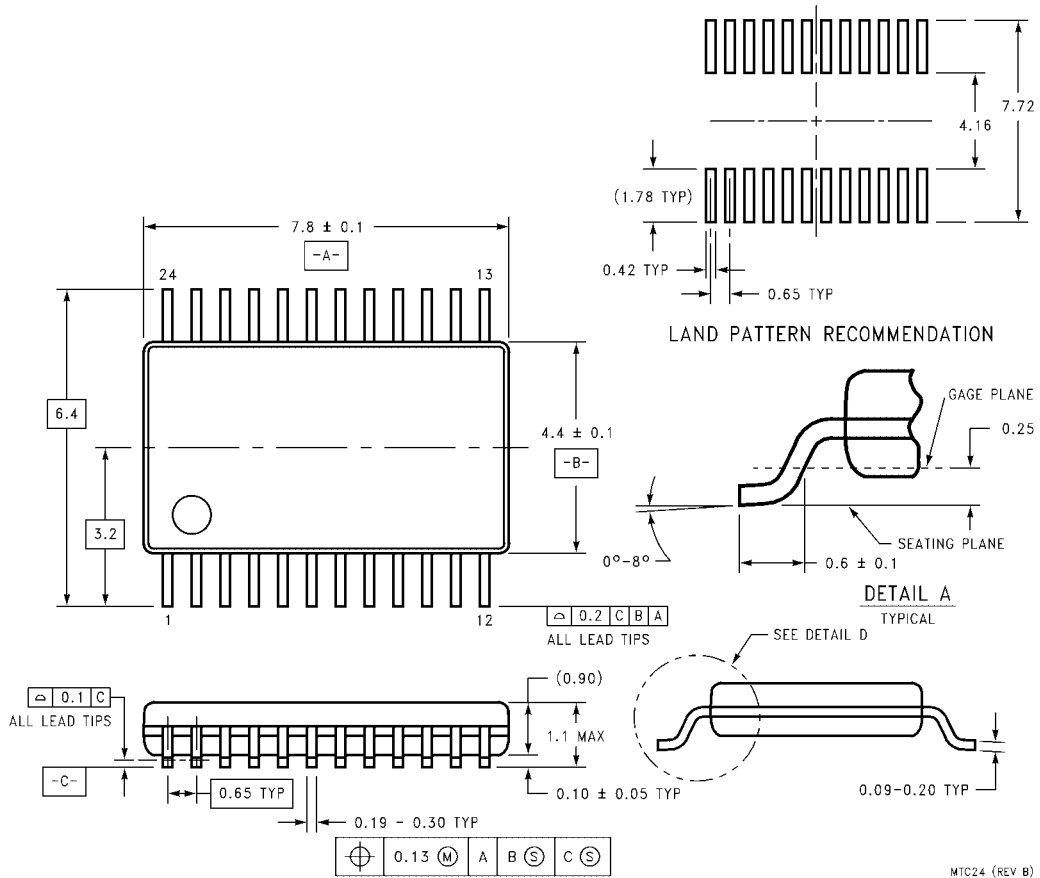
AC Electrical Characteristics								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 4)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	2.0	5.5	9.5	2.0	10.0	ns
t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	2.0	5.5	9.5	2.0	10.0	ns
t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	2.0	5.5	9.0	2.0	10.0	ns
t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	2.0	5.5	9.0	2.0	10.0	ns
t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to O <sub>n</sub>	5.0	2.0	5.5	9.5	2.0	10.5	ns
t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to O <sub>n</sub>	5.0	2.0	5.5	9.5	2.0	10.5	ns
t <sub>PHZ</sub>	Output Disable Time $\overline{OE}$ to O <sub>n</sub>	5.0	2.0	6.0	10.5	2.0	11.0	ns
t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to O <sub>n</sub>	5.0	2.0	6.0	10.5	2.0	11.0	ns
<b>Note 4:</b> Voltage Range 5.0 is 5.0V ± 0.5V								
AC Operating Requirements								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units	
			Typ	Guaranteed Minimum				
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	5.0	-0.5	0.5	1.0		ns	
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	5.0	0.5	2.0	2.0		ns	
t <sub>W</sub>	LE Pulse Width, HIGH	5.0	2.0	3.5	3.5		ns	
<b>Note 5:</b> Voltage Range 5.0 is 5.0V ± 0.5V								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN				
C <sub>PD</sub>	Power Dissipation Capacitance	44	pF	V <sub>CC</sub> = 5.0V				

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**

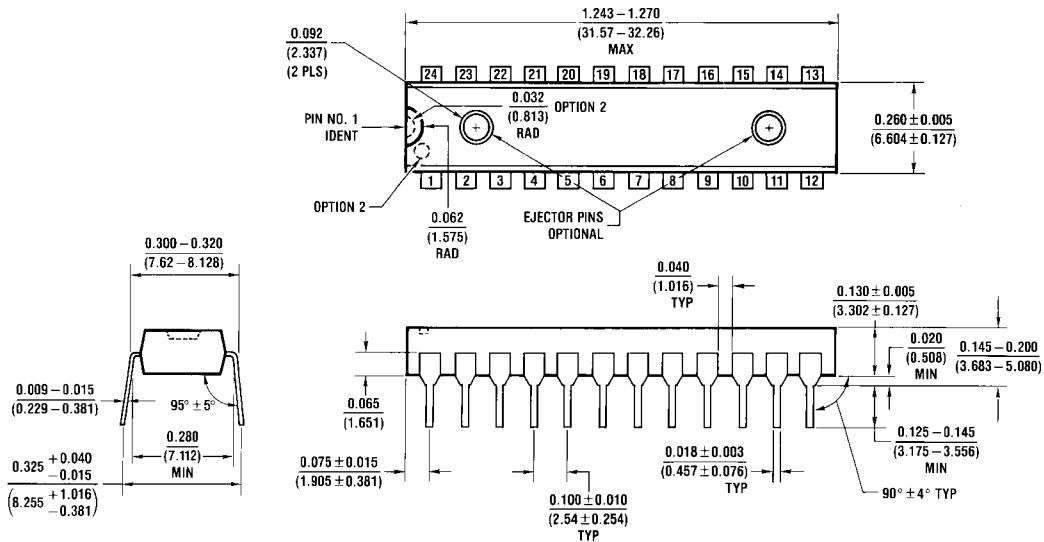
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
 Package Number MTC24**

MTC24 (REV B)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C**

N24C (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)