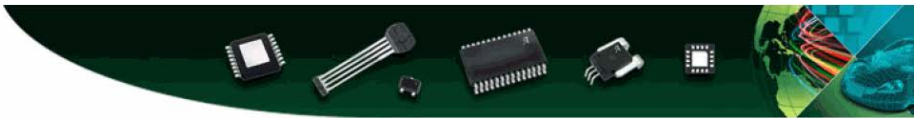

PCN Number: MC040417
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Product/Process Change Notification (PCN)

Customer: Digi-Key **Date: 4/4/2017**

Customer Part # and/or Lot# affected: A6263KLJTR-T

Originator: Mark Caggiano **Phone: 508-854-5603**

Duration of Change: Permanent [X] Temporary (explain) [ ]

Summary description of change: Part Change: [ ] Process Change: [X] Other: [ ]

1. Allegro currently manufactures the A6263KLJTR-T at wafer fab, Polar Semiconductor LLC. (PSL), Bloomington, MN, USA using ABCD5-8 technology. We will add a second source wafer fab known as United Microelectronics Corporation (UMC), Hsinshu, Taiwan using ABCD5-8 technology.
2. The above listed device will have an additional final test location: Allegro MicroSystems (Thailand) Co., Ltd. (AMTC).

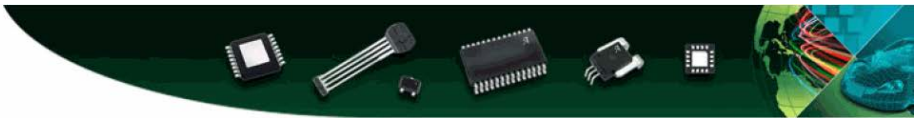
What is the part or process changing from (provide details)?

1. Allegro currently manufactures the A6263KLJTR-T at wafer fab, Polar Semiconductor LLC. (PSL), Bloomington, MN, USA using ABCD5-8 technology.
2. In addition to the current Allegro MicroSystems Philippines, Inc. (AMPI) test facility location, located in Manila, Philippines, a second test facility referred to as Allegro MicroSystems (Thailand) Co., Ltd. (AMTC) located in Saraburi, Thailand will be added as a primary site.

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

1. The A6263KLJTR-T will have a second source wafer fab known as United Microelectronics Corporation (UMC), Hsinshu, Taiwan using ABCD5-8 technology.
2. Allegro will be expanding its manufacturing capabilities with the addition of a new, whollyowned integrated circuit test facility located in Saraburi, Thailand. The same make and model test equipment will be utilized and test site transfer buy off data will be on file for each device before production begins.

Note: Validation of equivalence within a specific application is at the discretion of the Customer



High-Performance Semiconductors

Reliability Qualification Results

Device: **9263 (UMC version of the 6263)**
Assy Lot #: **1546102UAAA**
Fab Location: **UMC**
Package: **LJ (eSOIC)**

Number of Leads: **8**
Assembly Location: **Unisem**
Tracking Number: **3255**
Lead Finish: **100% Tin**

Reason For Qualification: ***9263*** **(UMC version of the 6263)** - ***Automotive Stop/Tail LED Array Driver***

Reliability Qualification Results

9263, STR#3255

Stress Test	Abv.	Test #	Test Method	Test Conditions	Requirements S.S.	Requirements Results
Preconditioning	PC	A1	JESD22-A113 / J-STD-020	85°C/60% RH, 168 hrs, Peak Reflow=260°C; MSL2, (HAST, AC, TC)	231	0 Rejects
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 60% RH, 0, 96 hrs	77	0 Rejects
Autoclave	AC	A3	JESD22-A102	121°C, 100% RH, 15 PSIG, 0, 96 hrs	77	0 Rejects
Temperature Cycle	TC	A4	JESD22-A104	-65°C to +175°C, 0, 500, 1000 Cycles	77	0 Rejects
High Temperature Storage Life	HTSL	A6	JESD22-A103	175°C, 0, 1000 hrs	77	0 Rejects
High Temperature Operating Life	HTOL	B1	JESD22-A108	150°C, 0, 1000 hrs	77	0 Rejects
Early Life Failure Rate	ELFR	B2	AEC-Q100-008 / JESD22-A108	150°C, 0, 48 hrs	800	0 Rejects
Wire Bond Shear	WBS	C1	JESD22-B116 / Q100-001	Test Conditions, Sampling Size are defined in the Test Method (Performed at Assembly location)		>25g (Minimum shear strength), 0 Rejects; Cpk>1.67
Wire Bond Pull	WBP	C2	Mil-Std-883 Method 2011, AEC-Q003	Temp conditions and sample size are defined in the test method. (Performed after TC)		0 Rejects; Cpk>1.67
Electrostatic Discharge Human Body Model	HBM	E2	AEC-Q100-002	Test Conditions, Sampling Size are defined in the Test Method		Classification H2, HBM = 2.5 kV
Electrostatic Discharge Charged Device Model	CDM	E3	AEC-Q100-011	Test Conditions, Sampling Size are defined in the Test Method		Classification = C6, = 1kV
Latch-Up	LU	E4	JESD78	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions - 30 pcs		0 Rejects; Cpk>1.67

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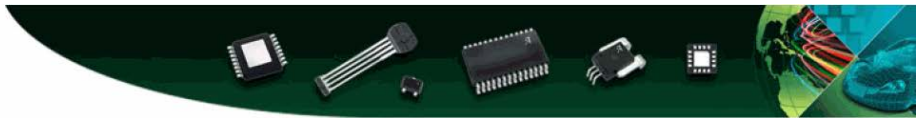
Is a PPAP update required? Yes [ ] No [X]

Is reliability testing required?
(If Yes, refer to attached plan) Yes [X] No (explain) [ ]



Expected completion date for internal qualification: Complete

Expected PPAP availability date: Available Upon Request

Target implementation date: October 2017

Estimated date of first shipment: November 2018

Expected sample availability date: Available Upon Request

Customer Approval Required:	**Yes**	☐	**Date Required:**
	No	X	**Notification Only**

Please note: It is our intention to inform our customer of changes as early as possible. Under Allegro's procedure for product/process change notification, Allegro strives, based on its technical judgment, to provide notification of significant changes that may affect form, fit or function. However, as Allegro cannot ensure evaluation of product/process changes for each and every application; the customer retains responsibility to validate the impact of a change on its application suitability. If samples are needed for validation of a change, requests may be made via the contact information provided herein. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled.

Customer comments/Conditions of Acceptance:

Approved by: Date: Title:

cc: Allegro Sales/Marketing/Quality