

P-Channel 1.8-V (G-S) MOSFET

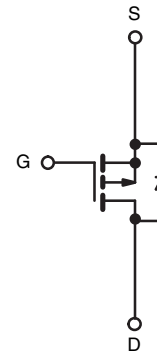
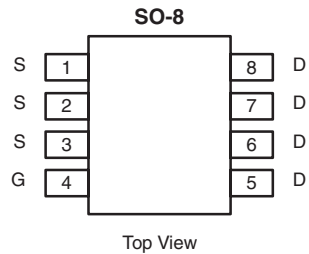
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^b	Q_g (Typ.)
- 8	0.009 at $V_{GS} = - 4.5$ V	- 13.7	55 nC
	0.011 at $V_{GS} = - 2.5$ V	- 12.4	
	0.016 at $V_{GS} = - 1.8$ V	- 10	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- 1.8 V Rated
- 100 % R_g Tested



RoHS
COMPLIANT
HALOGEN
FREE
Available



P-Channel MOSFET

Ordering Information: Si4465ADY-T1-E3 (Lead (Pb)-free)
Si4465ADY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 8	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150$ °C) ^{a, b}	I_D	$T_A = 25$ °C	- 13.7	A
		$T_A = 70$ °C	- 11	
		$T_C = 25$ °C	- 20	
		$T_C = 70$ °C	- 16	
Pulsed Drain Current	I_{DM}	- 40		
Continuous Source Current (Diode Conduction) ^{a, b}	I_S	- 2.5		
	I_{SM}	40		
Maximum Power Dissipation ^{a, b}	P_D	$T_A = 25$ °C	3.0	W
		$T_A = 70$ °C	1.95	
		$T_C = 25$ °C	6.5	
		$T_C = 70$ °C	4.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient (MOSFET) ^a	R_{thJA}	$t \leq 10$ s	34	41	°C/W
		Steady State	67	80	
Maximum Junction-to-Foot (Drain)	R_{thJF}	15	19		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t \leq 10$ s.

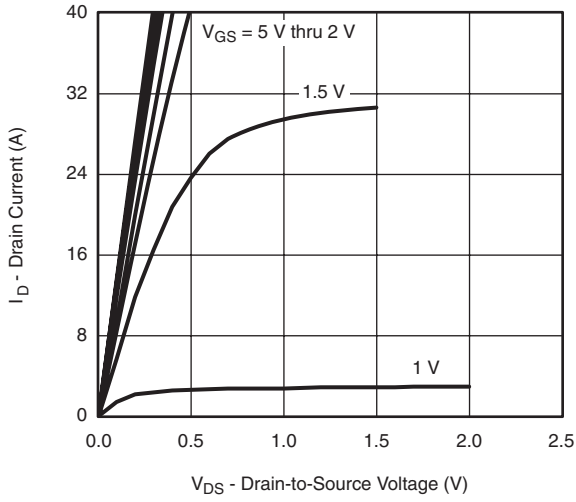
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	- 0.45		- 1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -8\text{ V}$, $V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -8\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			- 5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	- 20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$		0.0075	0.009	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -12\text{ A}$		0.0092	0.011	
		$V_{GS} = 1.8\text{ V}$, $I_D = 10\text{ A}$		0.013	0.016	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}$, $I_D = -14\text{ A}$		58		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.1\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.57	- 1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -4\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$		55	85	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			10		
Gate Resistance	R_g			2.5	3.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong -10\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 6\text{ }\Omega$		33	50	ns
Rise Time	t_r			170	255	
Turn-Off Delay Time	$t_{d(off)}$			168	255	
Fall Time	t_f			112	170	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		85	130	nC
Body Diode Reverse Recovery Charge	Q_{rr}			81	125	

Notes:

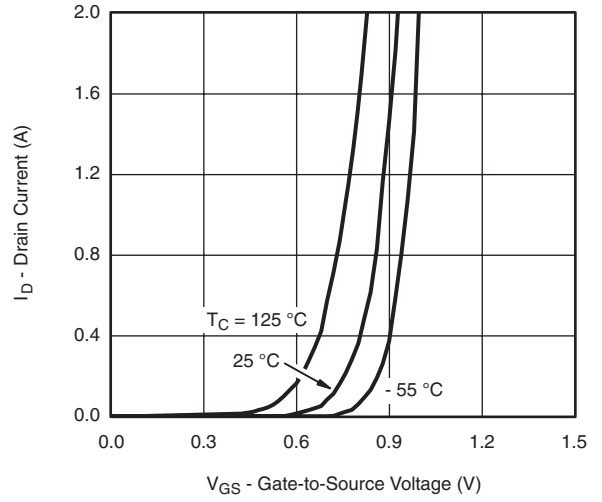
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

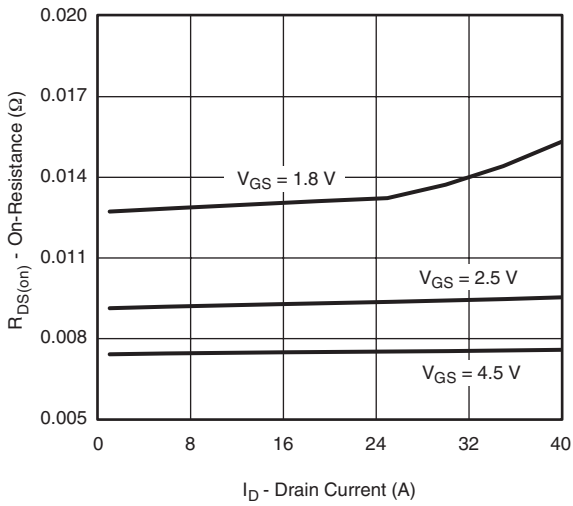
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



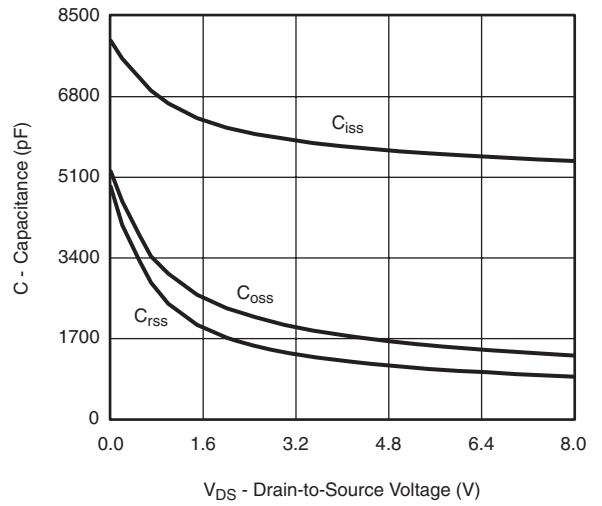
Output Characteristics



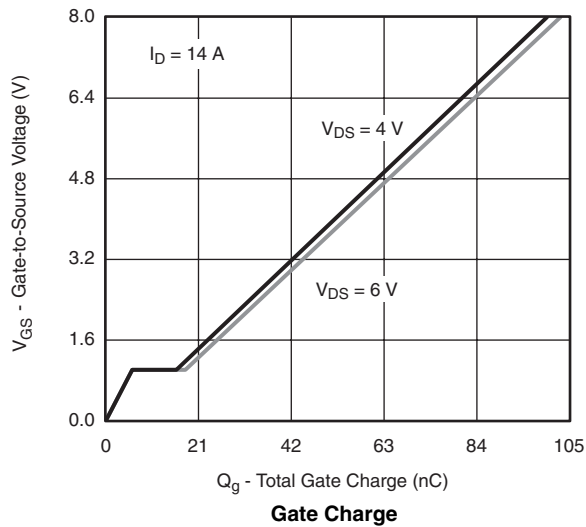
Transfer Characteristics



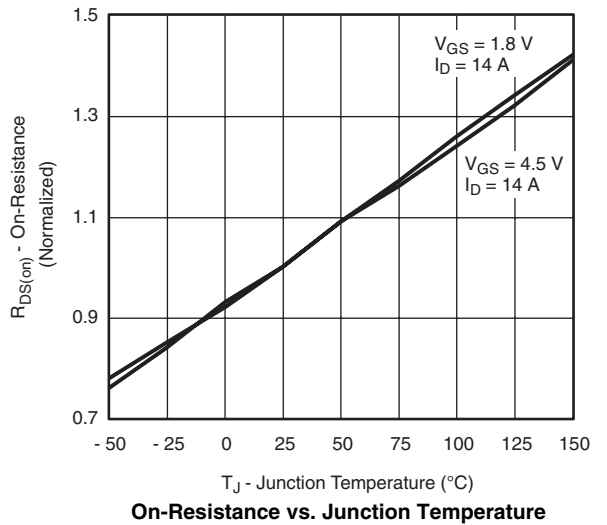
On-Resistance vs. Drain Current



Capacitance

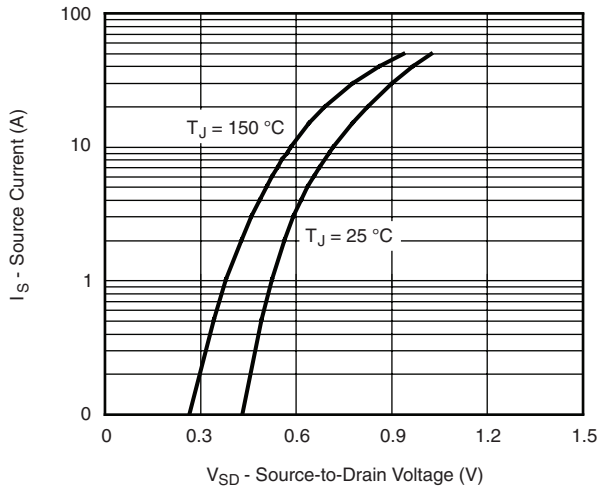


Gate Charge

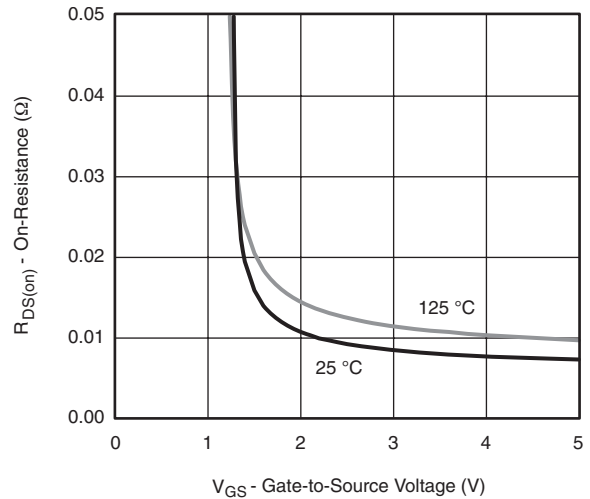


On-Resistance vs. Junction Temperature

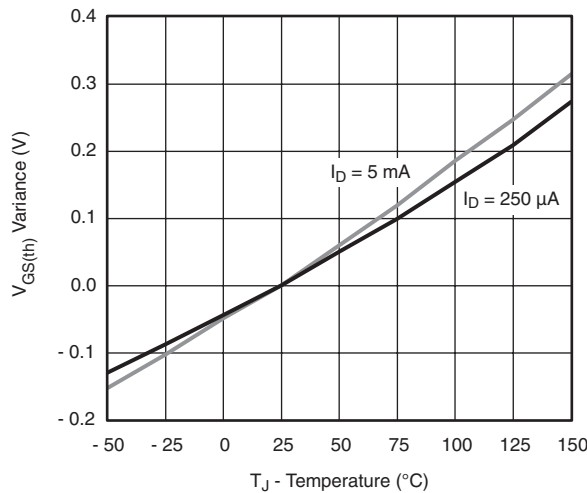
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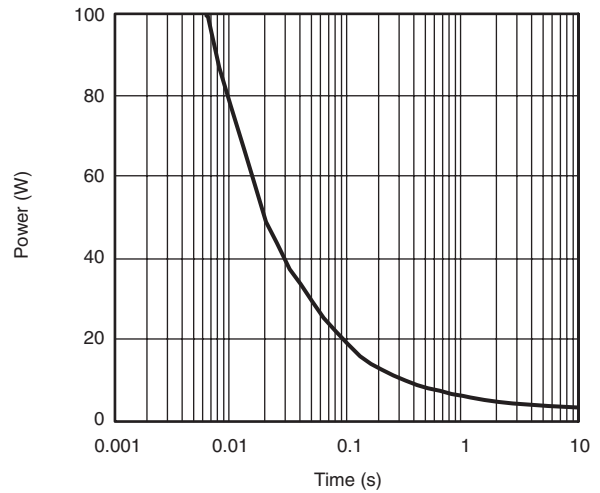
Source-Drain Diode Forward Voltage



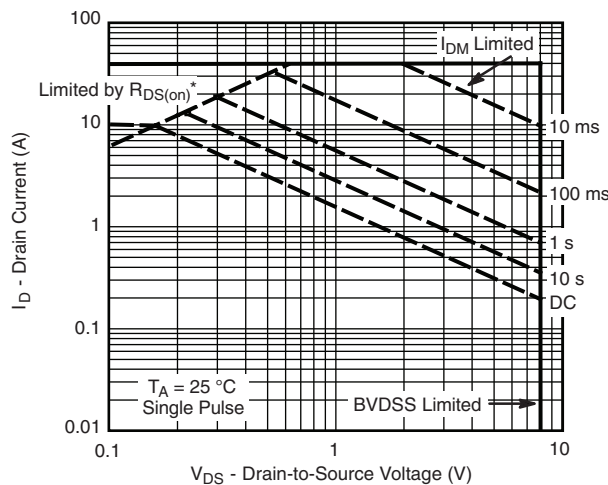
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



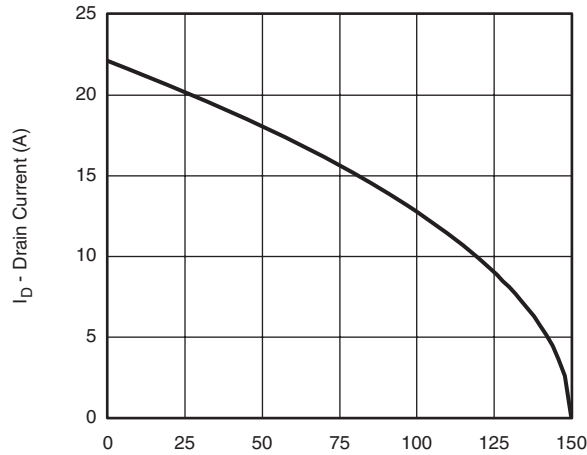
Single Pulse Power, Junction-to-Ambient



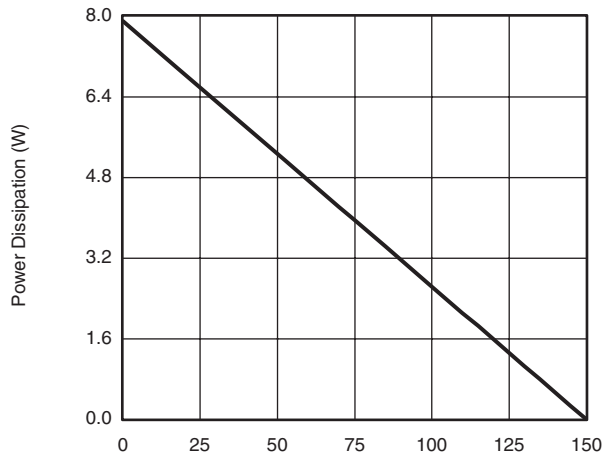
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operatin Area

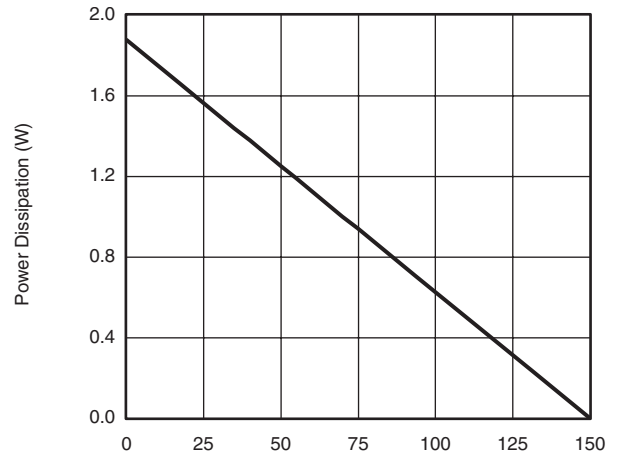
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)
Current Derating



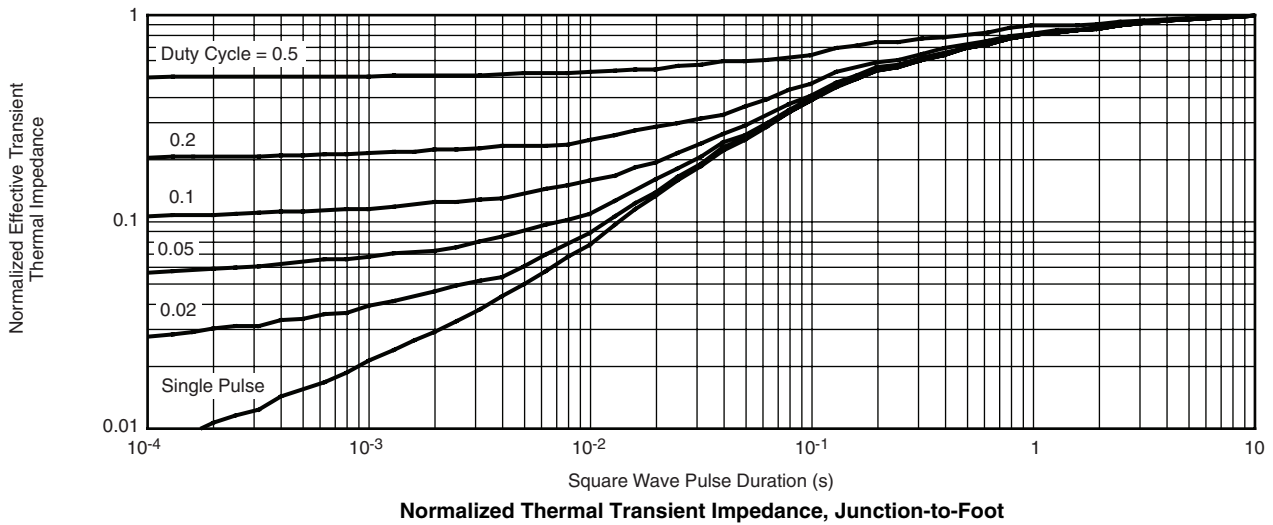
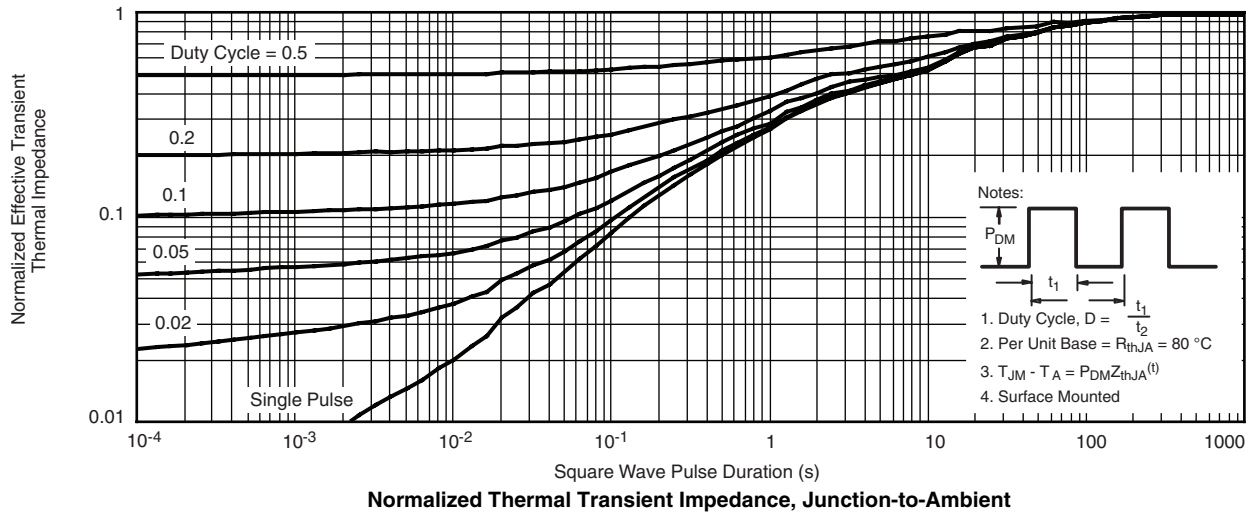
T_C - Case Temperature (°C)
Power, Junction-to-Foot



T_A - Ambient Temperature (°C)
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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