

P-channel 500 V, 3 Ω typ., 2.8 A Zener-protected SuperMESH™ Power MOSFET in a DPAK package

Datasheet - production data

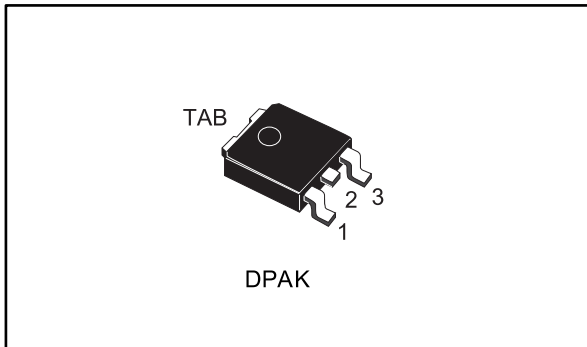


Figure 1: Internal schematic diagram

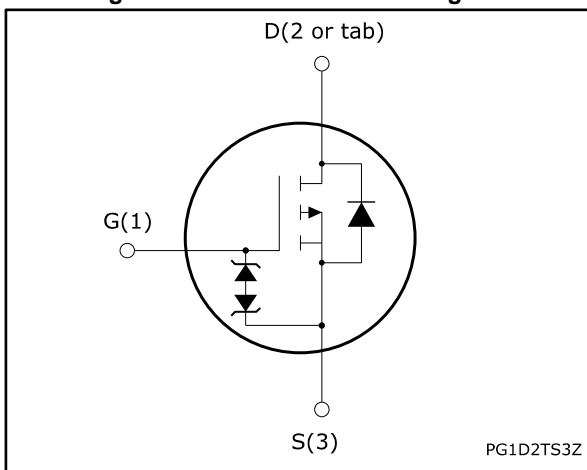


Table 1: Device summary

Order code	Marking	Package	Packing
STD3PK50Z	3PK50Z	DPAK	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STD3PK50Z	500 V	4 Ω	2.8 A	70 W

- Gate charge minimized
- Extremely high dv/dt capability
- 100% avalanche tested
- Very low intrinsic capacitance
- Improved ESD capability

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected P-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.



For the P-channel Power MOSFET, current and voltage polarities are reversed.

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1 Electrical ratings



For the P-channel Power MOSFET, current and voltage polarities are reversed.

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.8	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	11	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	85	W
I_{AS}	Single-pulse avalanche current (pulse width limited by T_{jmax})	2.8	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	200	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	3	kV
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾ $I_{SD} \leq 2.8\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD(peak)} \leq V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.47	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb	50	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)



For the P-channel Power MOSFET, current and voltage polarities are reversed.

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ }^\circ\text{C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.4\text{ A}$		3	4	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	530	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }400\text{ V}$	-	32	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	23	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4.7	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 2.8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14: "Gate charge test circuit")	-	29	-	nC
Q_{gs}	Gate-source charge		-	4.3	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

Notes:

⁽¹⁾ $C_{o(tr)}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

⁽²⁾ $C_{o(er)}$ is defined as the constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 1.4\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load")	-	16	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	46	-	ns
t_f	Fall time		-	26	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.8	A
I_{SDM}	Source-drain current (pulsed)				11.2	A
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 35\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.8\text{ A}$, $V_{DD} = 60\text{ V}$, $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	220		ns
Q_{rr}	Reverse recovery charge		-	1.6		μC
I_{RRM}	Reverse recovery current		-	14		A
t_{rr}	Reverse recovery time	$I_{SD} = 2.8\text{ A}$, $V_{DD} = 60\text{ V}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.1		μC
I_{RRM}	Reverse recovery current		-	15		A

Notes:

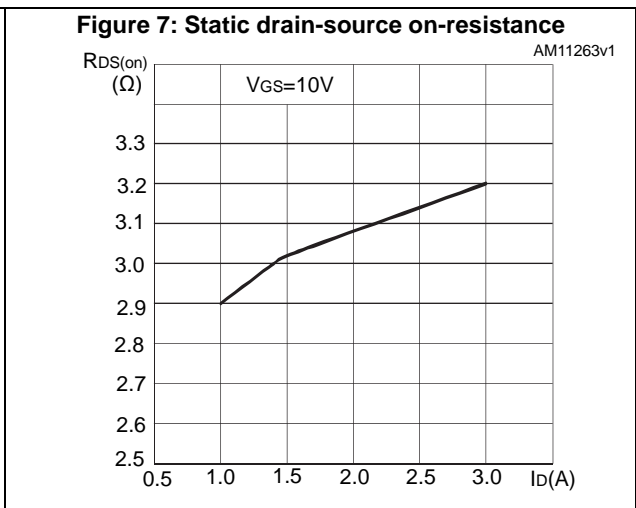
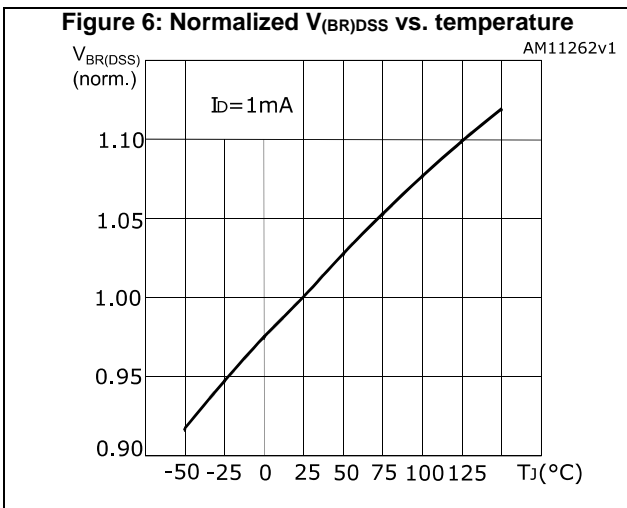
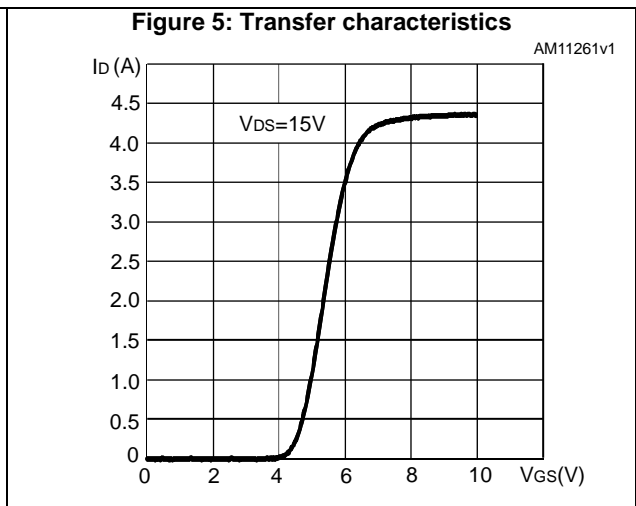
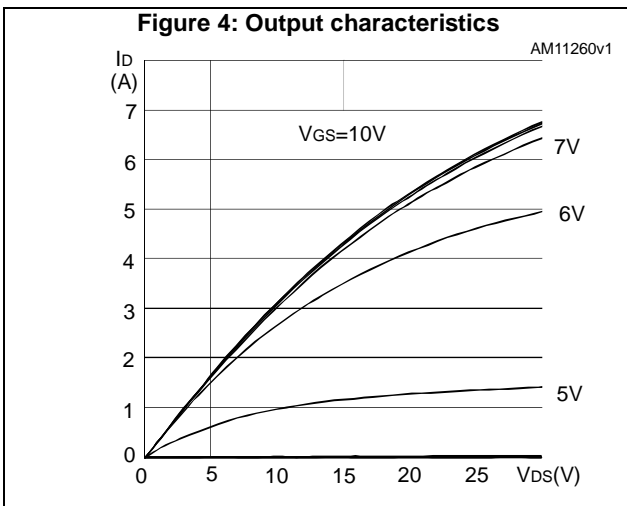
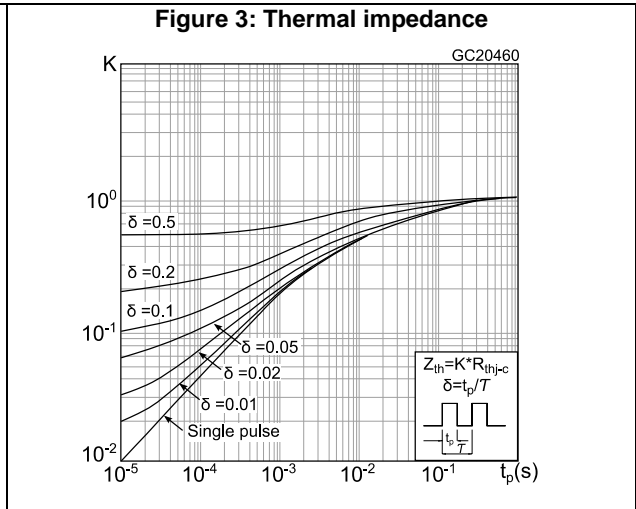
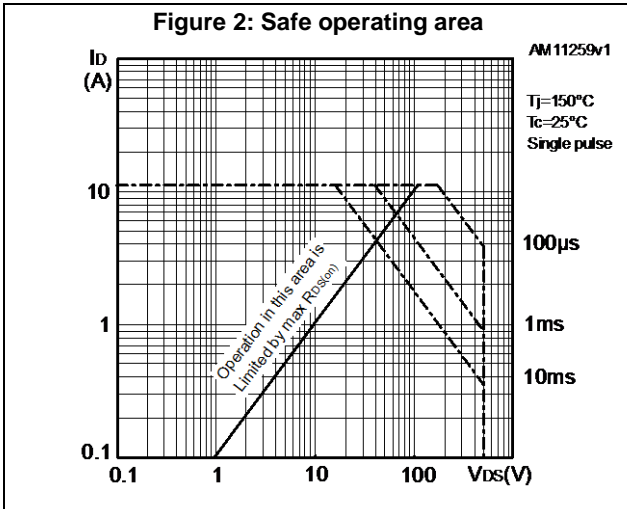
⁽¹⁾Pulse test: pulse duration = 300 μs , duty cycle 1.5%

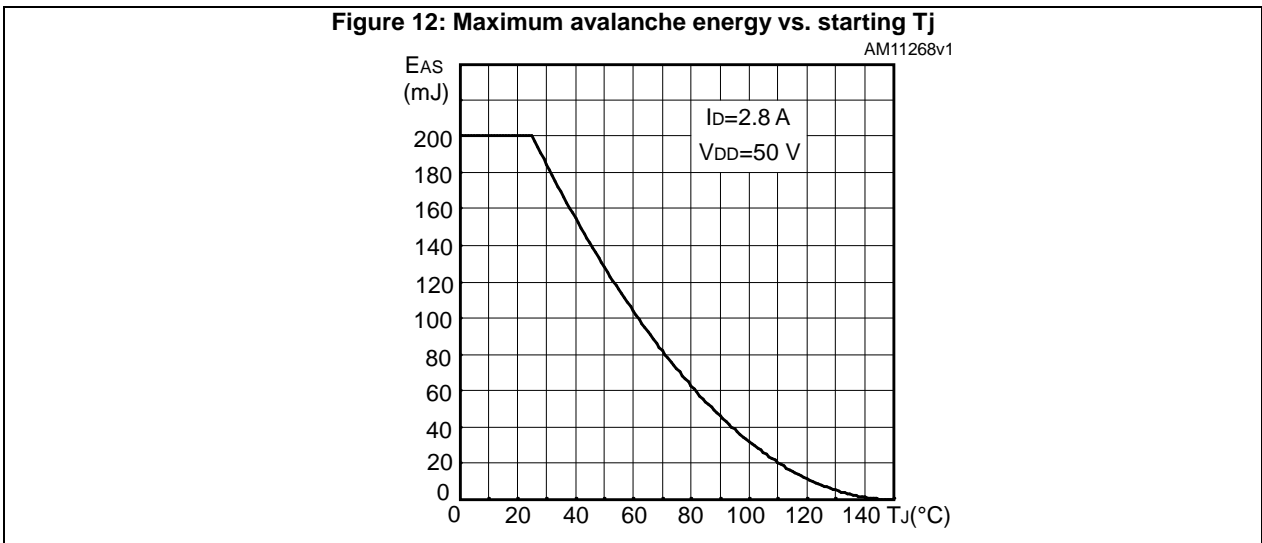
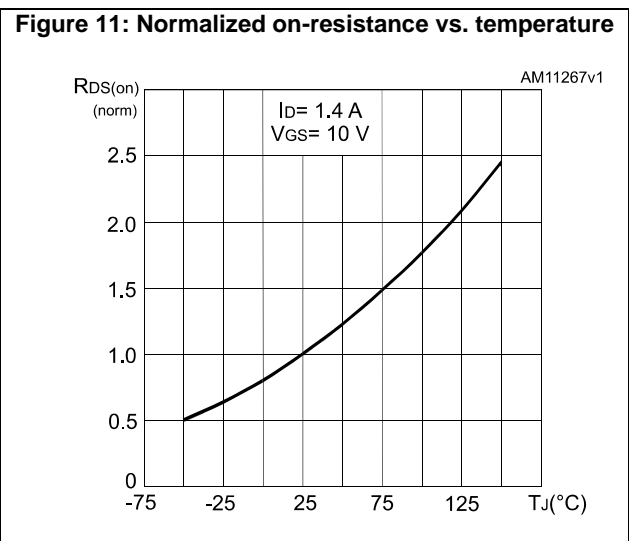
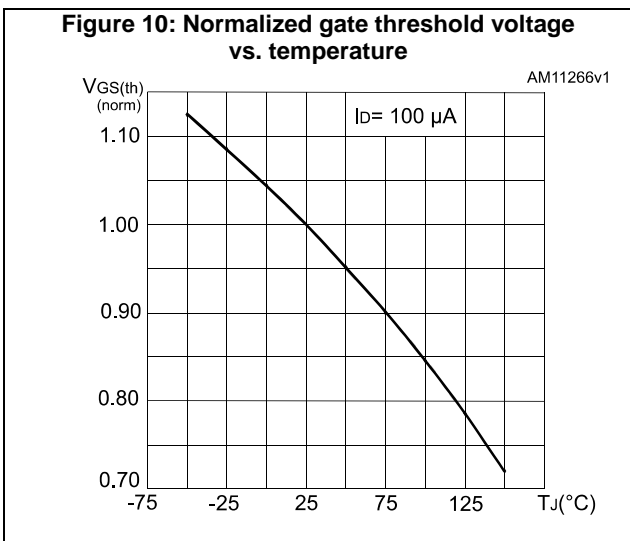
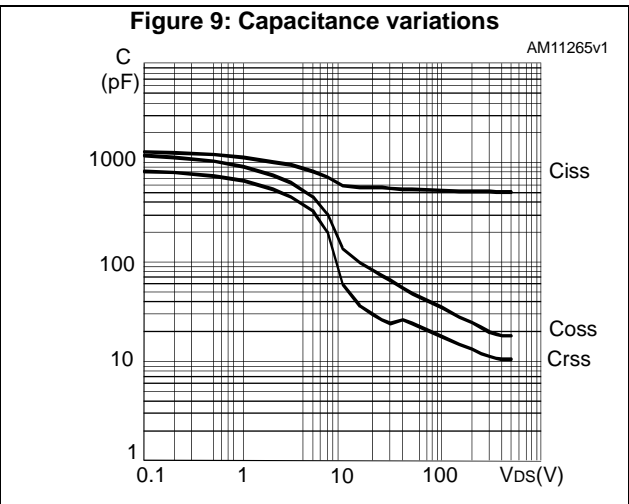
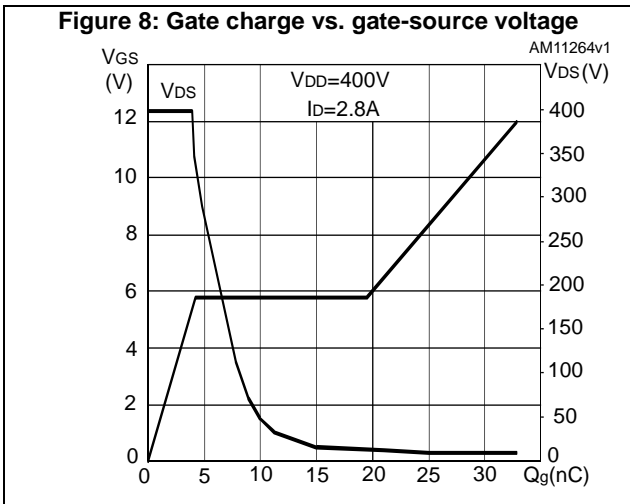
Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Switching times test circuit for resistive load

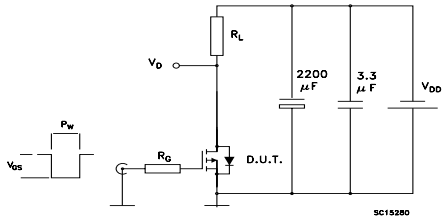


Figure 14: Gate charge test circuit

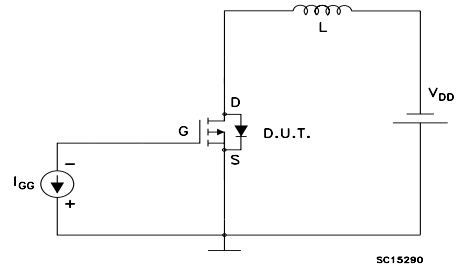
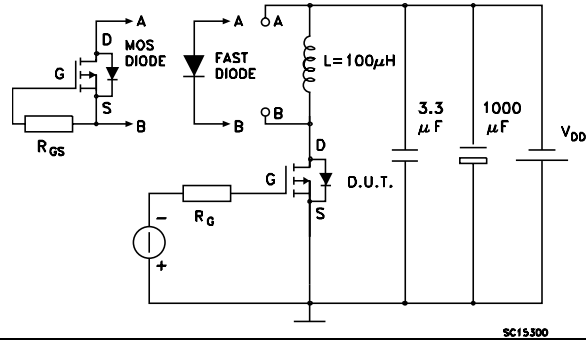


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK package information

Figure 16: DPAK (TO-252) type A package outline

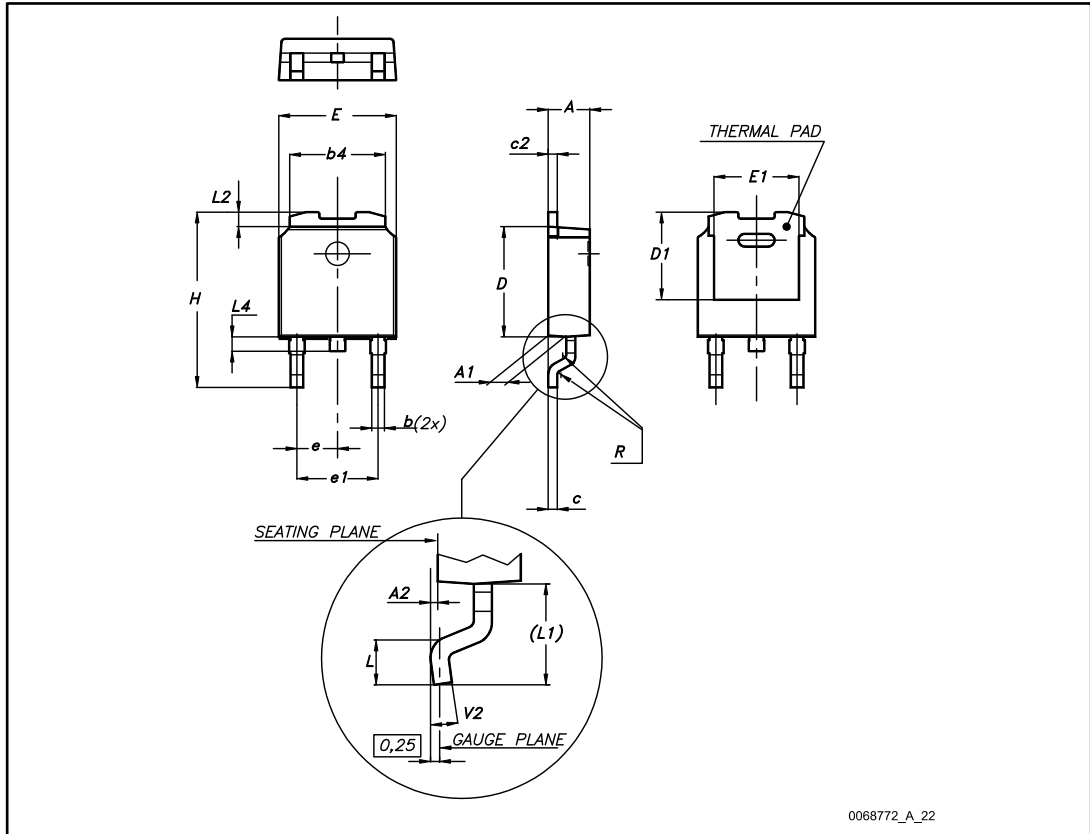
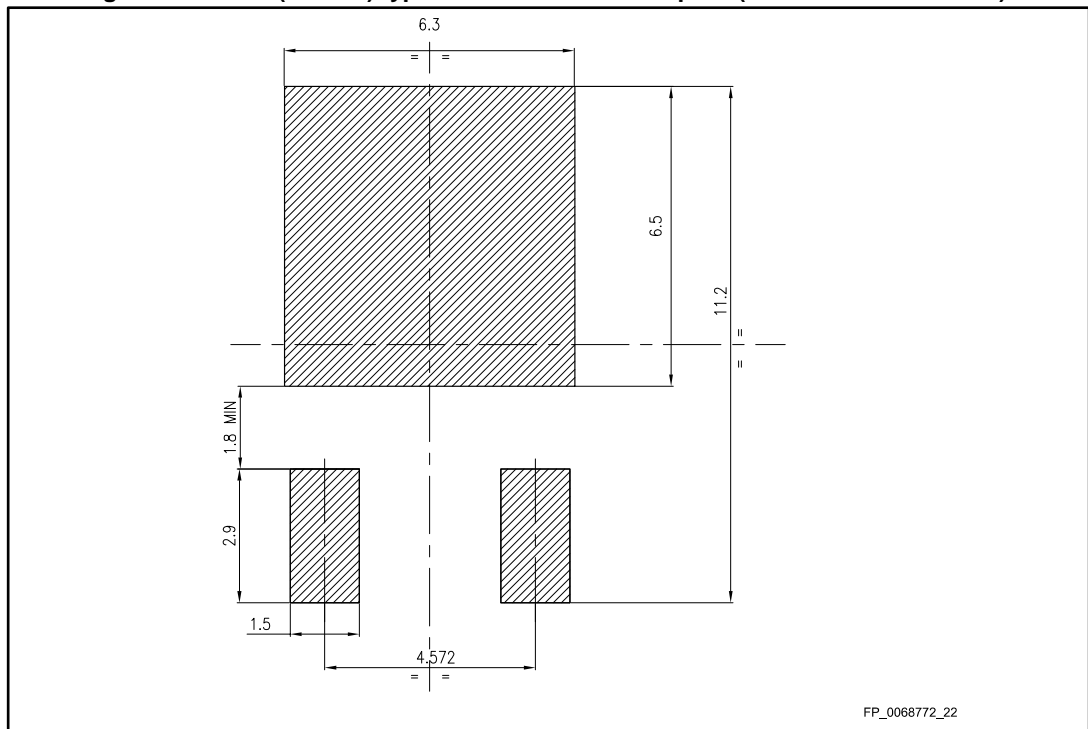


Table 9: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) type A recommended footprint (dimensions are in mm)



4.2 DPAK packing information

Figure 18: DPAK (TO-252) tape outline

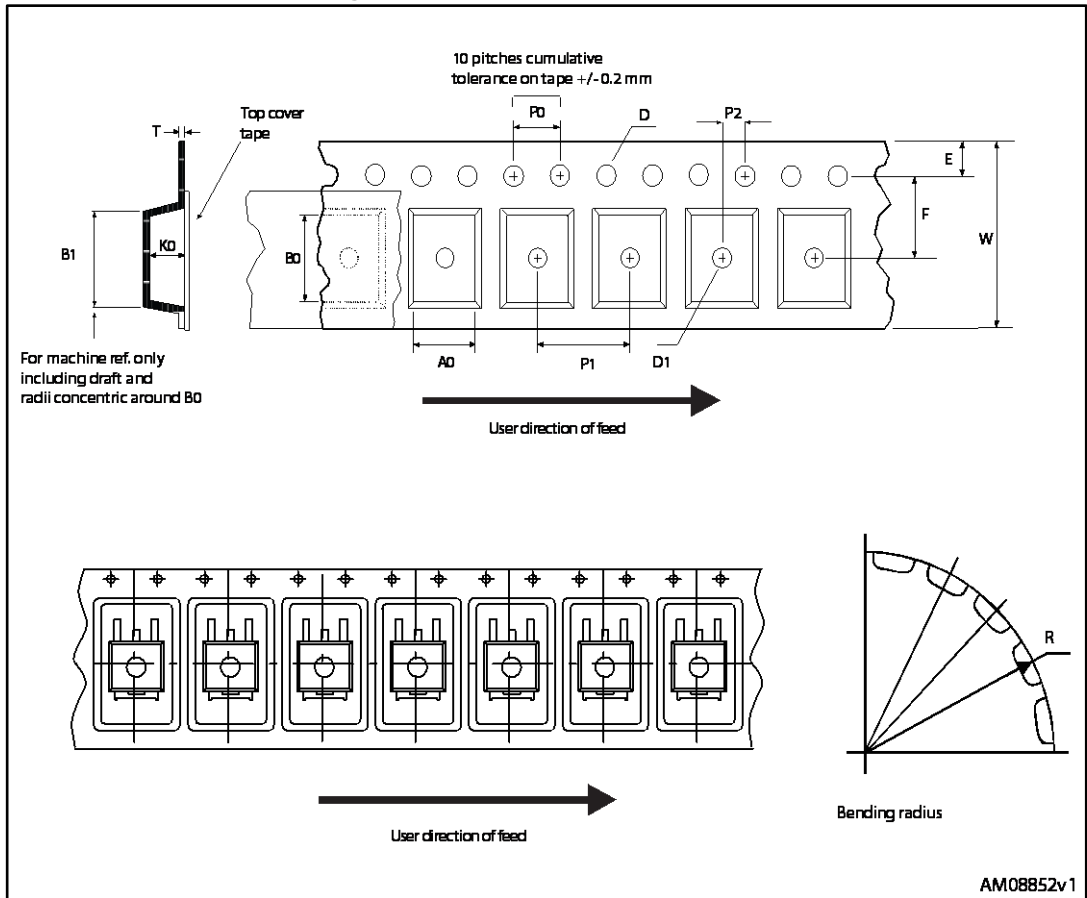


Figure 19: DPAK (TO-252) reel outline

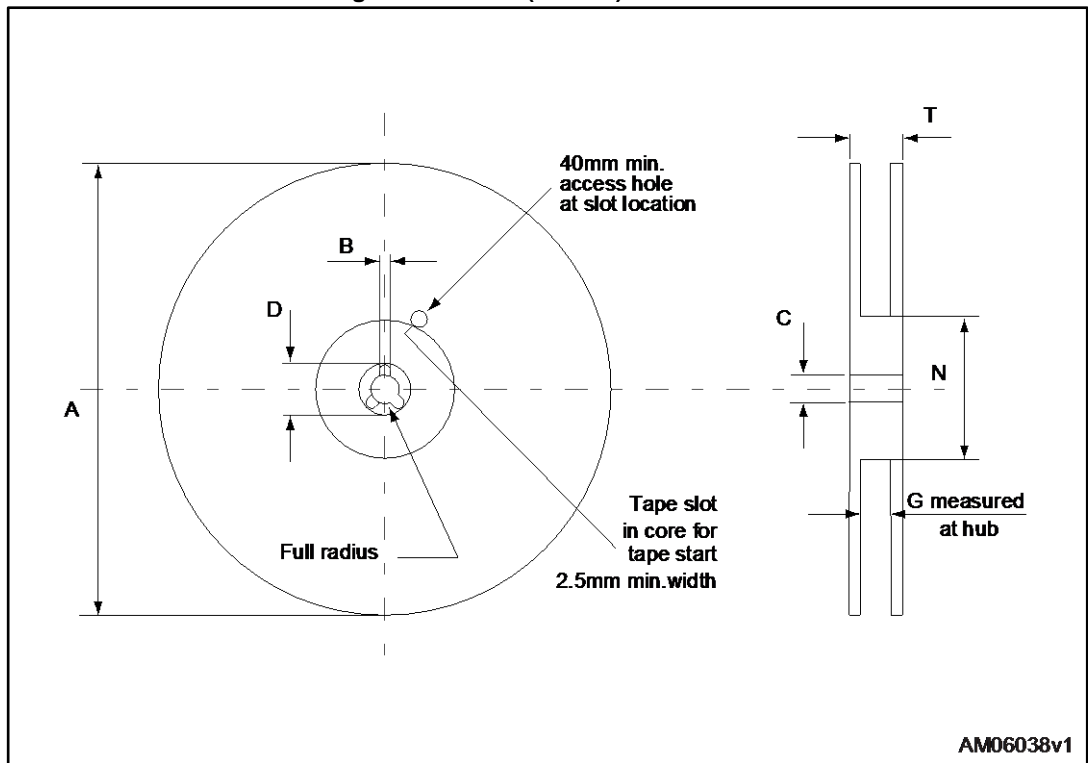


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Nov-2010	1	First release.
31-Aug-2012	2	Document status promoted from preliminary data to production data. Minor text changes on the cover page.
05-May-2017	3	Updated Table 7: "Source drain diode" . Minor text changes

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