19-2012; Rev 2; 4/03

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs and Disable

General Description

The MAX4380–MAX4384 family of op amps are unity-gain-stable devices that combine high-speed performance, Rail-to-Rail® outputs, and high-impedance disable mode. These devices operate from a +4.5V to +11V single supply or from ±2.25V to ±5.5V dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

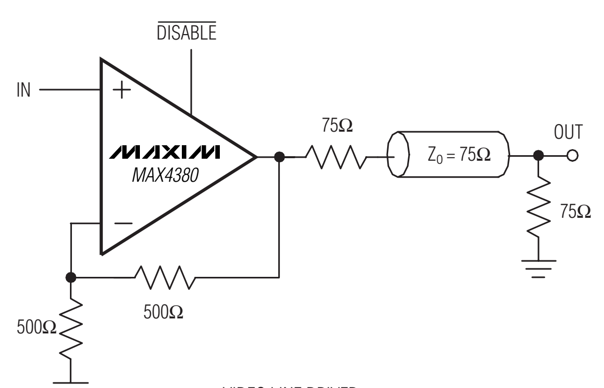
The MAX4380–MAX4384 require only 5.5mA of quiescent supply current per op amp while achieving a 210MHz -3dB bandwidth, 55MHz 0.1dB gain flatness and a 485V/µs slew rate. These devices are an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation.

The MAX4380 single with disable is available in an ultra-small 6-pin SC70 package.

Applications

Set-Top Boxes
Surveillance Video Systems
Battery-Powered Instruments
Analog-to-Digital Converter Interface
CCD Imaging Systems
Video Routing and Switching Systems
Digital Cameras
Video-on-Demand
Video Line Driver

Typical Operating Circuit



VIDEO LINE DRIVER

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

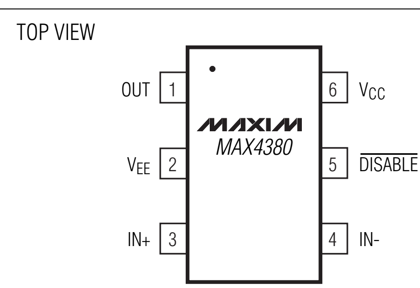
Features

- ♦ **Low Cost and High Speed:**
  - **210MHz -3dB Bandwidth**
  - **55MHz 0.1dB Gain Flatness**
  - **485V/µs Slew Rate**
- ♦ **Disable Mode Places Outputs in High-Impedance State**
- ♦ **Single +4.5V to +11V Operation**
- ♦ **Rail-to-Rail Outputs**
- ♦ **Input Common-Mode Range Extends Beyond V_{EE}**
- ♦ **Low Differential Gain/Phase: 0.02%/0.08°**
- ♦ **Low Distortion at 5MHz**
  - **-65dBc SFDR**
  - **-63dB Total Harmonic Distortion**
- ♦ **Ultra-Small 6-Pin SC70, 6-Pin SOT23, 10-Pin µMAX, 14-Pin TSSOP, and 20-Pin TSSOP Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4380EXT-T	-40°C to +85°C	6 SC70-6	AAV
MAX4380EUT-T	-40°C to +85°C	6 SOT23-6	—
MAX4381EUB	-40°C to +85°C	10 µMAX	—
MAX4382EUD	-40°C to +85°C	14 TSSOP	—
MAX4382ESD	-40°C to +85°C	14 SO	—
MAX4382EEE	-40°C to +85°C	16 QSOP	—
MAX4383EUD	-40°C to +85°C	14 TSSOP	—
MAX4383ESD	-40°C to +85°C	14 SO	—
MAX4383ESE	-40°C to +85°C	16 SO	—
MAX4383EEE	-40°C to +85°C	16 QSOP	—
MAX4384EUP	-40°C to +85°C	20 TSSOP	—

Pin Configurations



SC70-6/SOT23-6

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})..+12V
IN_-, IN_+, OUT_, $\overline{\text{DISABLE}}$_ ....($V_{EE}$ - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit to V_{CC} or V_{EE} 1s
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
6-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C).........727mW
14-Pin SO (derate 8.3mW/°C above +70°C) 667mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) ..696mW
20-Pin TSSOP (derate 10.9mW/°C above +70°C).......879mW
Operating Temperature Range. ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or at any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS–Single Supply

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = V_{CC}/2, V_{OUT} = V_{CC}/2, R_L = ∞ to V_{CC}/2, $\overline{\text{DISABLE}}$_ = V_{CC} (MAX4380/MAX4381/MAX4382/MAX4384), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR		V_{EE} - 0.2		V_{CC} - 2.25	V
Input Offset Voltage	V_{OS}	T_A = +25°C			0.2	12	mV
		T_A = -40°C to +85°C				20	
Input Offset Voltage Matching		MAX4381–MAX4384			1		mV
Input Offset Voltage Tempco	TC_{VOS}				8		µV/°C
Input Bias Current	I_B				6.5	20	µA
Input Offset Current	I_{OS}				0.5	7	µA
Input Resistance	R_{IN}	Differential mode (-1V ≤ V_{IN} ≤ +1V)			70		kΩ
		Common mode (-0.2V ≤ V_{CM} ≤ +2.75V)			3		MΩ
Common-Mode Rejection Ratio	CMRR	V_{EE} - 0.2V ≤ V_{CM} ≤ V_{CC} - 2.25V		70	95		dB
Open-Loop Gain	A_{VOL}	0.25V ≤ V_{OUT} ≤ 4.75V, R_L = 2kΩ		50	61		dB
		0.8V ≤ V_{OUT} ≤ 4.5V, R_L = 150Ω		48	63		
		1V ≤ V_{OUT} ≤ 4V, R_L = 50Ω			58		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	V_{CC} - V_{OH}		0.05	0.2	V
			V_{OL} - V_{EE}		0.05	0.15	
		R_L = 150Ω	V_{CC} - V_{OH}		0.3	0.5	
			V_{OL} - V_{EE}		0.25	0.8	
		R_L = 75Ω	V_{CC} - V_{OH}		0.5	0.8	
			V_{OL} - V_{EE}		0.5	1.75	
		R_L = 75Ω to ground	V_{CC} - V_{OH}		1	1.7	
			V_{OL} - V_{EE}		0.025	0.125	
Output Current	I_{OUT}	Sinking from R_L = 75Ω to V_{CC}		40	55		mA
		Sourcing into R_L = 75Ω to V_{EE}		25	50		
Output Short-Circuit Current	I_{SC}	Sinking or sourcing			±100		mA
Open-Loop Output Resistance	R_{OUT}				8		Ω
Power-Supply Rejection Ratio	PSRR	V_S = +4.5V to +5.5V		50	62		dB

DC ELECTRICAL CHARACTERISTICS–Single Supply

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = V_{CC}/2, V_{OUT} = V_{CC}/2, R_L = ∞ to V_{CC}/2, $\overline{DISABLE\_}$ = V_{CC} (MAX4380/MAX4381/MAX4382/MAX4384), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_S	Guaranteed by PSRR (Note 2)	4.5		11	V
Disabled Output Resistance	$R_{OUT(OFF)}$	$\overline{DISABLE\_}$ = 0, 0 ≤ V_{OUT} ≤ 5V	27	35		kΩ
$\overline{DISABLE\_}$ Logic-Low Threshold	V_{IL}				V_{CC} - 3	V
$\overline{DISABLE\_}$ Logic-High Threshold	V_{IH}		V_{CC} - 1.25			V
$\overline{DISABLE\_}$ Logic Input Low Current	I_{IL}	$\overline{DISABLE\_}$ = 0		25	60	µA
$\overline{DISABLE\_}$ Logic Input High Current	I_{IH}	$\overline{DISABLE\_}$ = V_{CC}		10	40	µA
Quiescent Supply Current (Per Amplifier)	I_S	$\overline{DISABLE\_}$ = V_{CC}		5.5	9	mA
		$\overline{DISABLE\_}$ = 0		0.45	0.6	

DC ELECTRICAL CHARACTERISTICS–Dual Supply

(V_{CC} = +5V, V_{EE} = -5V, V_{CM} = 0, V_{OUT} = 0, R_L = ∞ to 0, $\overline{DISABLE\_}$ = V_{CC} (MAX4380/MAX4381/MAX4382/MAX4384), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR		V_{EE}		V_{CC} - 2.25	V
Input Offset Voltage	V_{OS}	T_A = +25°C			3	16	mV
		T_A = T_{MIN} to T_{MAX}				24	
Input Offset Voltage Matching		MAX4381–MAX4384			1		mV
Input Offset Voltage Tempco	TC_{VOS}				8		µV/°C
Input Bias Current	I_B				8.5	25	µA
Input Offset Current	I_{OS}				0.5	12	µA
Input Resistance	R_{IN}	Differential mode (-1V ≤ V_{IN} ≤ +1V)			70		kΩ
		Common mode (-5V ≤ V_{CM} ≤ 2.75V)			3		MΩ
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ V_{CC} - 2.25V		70	95		dB
Open-Loop Gain	A_{VOL}	-4.5V ≤ V_{OUT} ≤ +4.5V, R_L = 2kΩ		50	62		dB
		-4.25V ≤ V_{OUT} ≤ +4.25V, R_L = 150Ω		48	65		
		-4V ≤ V_{OUT} ≤ +4V, R_L = 50Ω			60		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	V_{CC} - V_{OH}		0.175	0.375	V
			V_{OL} - V_{EE}		0.075	0.225	
		R_L = 150Ω	V_{CC} - V_{OH}		0.575	0.85	
			V_{OL} - V_{EE}		0.4	0.775	
		R_L = 75Ω	V_{CC} - V_{OH}		1.3	2.3	
			V_{OL} - V_{EE}		1.3	2.45	

DC ELECTRICAL CHARACTERISTICS–Dual Supply (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{CM} = 0, V_{OUT} = 0, R_L = ∞ to 0, $\overline{DISABLE\_}$ = V_{CC} (MAX4380/MAX4381/MAX4382/MAX4384), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current	I_{OUT}	Sinking from R_L = 75Ω to V_{CC}	50	75		mA
		Sourcing into R_L = 75Ω to V_{EE}	50	75		
Output Short-Circuit Current	I_{SC}	Sinking or sourcing		±100		mA
Open-Loop Output Resistance	R_{OUT}			8		Ω
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	48	62		dB
Operating Supply Voltage Range	V_S	Guaranteed by PSRR (Note 2)	±2.25		±5.5	V
Disabled Output Resistance	$R_{OUT(OFF)}$	$\overline{DISABLE\_}$ = 0, -5V ≤ V_{OUT} ≤ 5V	27	35		kΩ
$\overline{DISABLE\_}$ Logic-Low Threshold	V_{IL}				V_{CC} - 3	V
$\overline{DISABLE\_}$ Logic-High Threshold	V_{IH}		V_{CC} - 1.25			V
$\overline{DISABLE\_}$ Logic Input Low Current	I_{IL}	$\overline{DISABLE\_}$ = 0		25		µA
$\overline{DISABLE\_}$ Logic Input High Current	I_{IH}	$\overline{DISABLE\_}$ = V_{CC}		10		µA
Quiescent Supply Current (Per Amplifier)	I_S	$\overline{DISABLE\_}$ = V_{CC}		7.5	10	mA
		$\overline{DISABLE\_}$ = 0		0.45	0.8	

AC ELECTRICAL CHARACTERISTICS–Single Supply

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, R_L = 100Ω to V_{CC}/2, $\overline{DISABLE\_}$ = V_{CC} (MAX4380/MAX4381/MAX4382/MAX4384), V_{OUT} = V_{CC}/2, A_{VCL} = +1V/V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 100mVp-p			210		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p			175		MHz
Small-Signal 0.1dB Gain Flatness	$BW_{0.1dBSS}$	V_{OUT} = 100mVp-p			55		MHz
Large-Signal 0.1dB Gain Flatness	$BW_{0.1dBLS}$	V_{OUT} = 2Vp-p			40		MHz
Slew Rate	SR	V_{OUT} = 2V step			485		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			16		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 100mVp-p			4		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p			-65		dBc
Harmonic Distortion	HD	f_C = 5MHz, V_{OUT} = 2Vp-p	2nd harmonic		-65		dBc
			3rd harmonic		-68		
			Total harmonic		-63		
Two-Tone, Third-Order Intermodulation Distortion	IP3	f1 = 4.7MHz, f2 = 4.8MHz, V_{OUT} = 1Vp-p			-66		dBc

AC ELECTRICAL CHARACTERISTICS–Single Supply (continued)

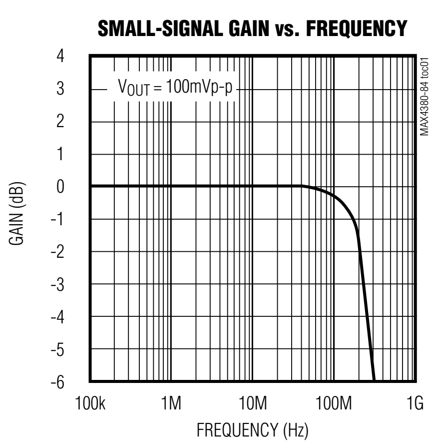
(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, R_L = 100Ω to V_{CC}/2, $\overline{DISABLE\_}$ = V_{CC} (MAX4380/MAX4381/MAX4382/MAX4384), V_{OUT} = V_{CC}/2, A_{VCL} = +1V/V, T_A = +25°C, unless otherwise noted.)

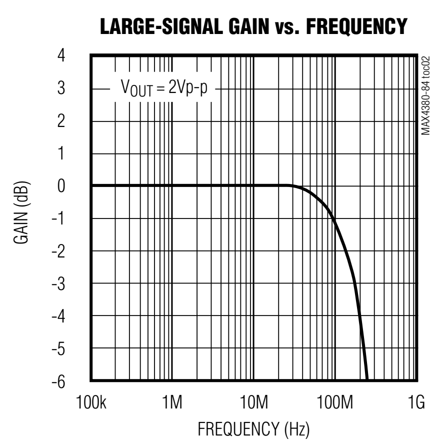
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Channel-to-Channel Isolation	CH_{ISO}	Specified at DC		-102		dB
Input 1dB Compression Point		f_C = 10MHz, A_{VCL} = +2V/V		14		dBm
Differential Phase Error	DP	NTSC, R_L = 150Ω		0.08		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω		0.02		%
Input Noise-Voltage Density	e_n	f = 10kHz		10		nV/√Hz
Input Noise-Current Density	I_n	f = 10kHz		2		pA/√Hz
Input Capacitance	C_{IN}			1		pF
Output Impedance	Z_{OUT}	f = 10MHz		1.5		Ω
Enable Time	t_{ON}	V_{IN} = 1V (MAX4380/MAX4381/ MAX4382/MAX4384)		100		ns
Disable Time	t_{OFF}	V_{IN} = 1V (MAX4380/MAX4381/ MAX4382/MAX4384)		1		µs

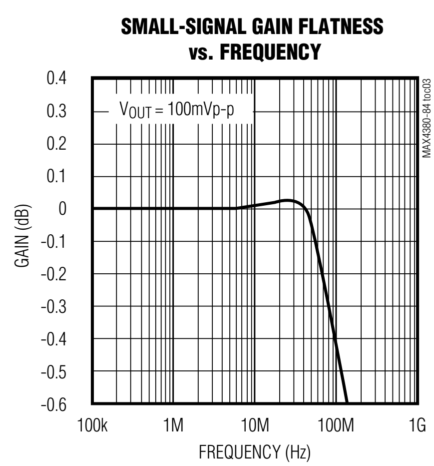
Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: PSRR for single +5V supply tested with V_{EE} = 0, V_{CC} = +4.5V to +5.5V; PSRR for dual ±5V supply tested with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V.

Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, A_{VCL} = +1V/V, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)



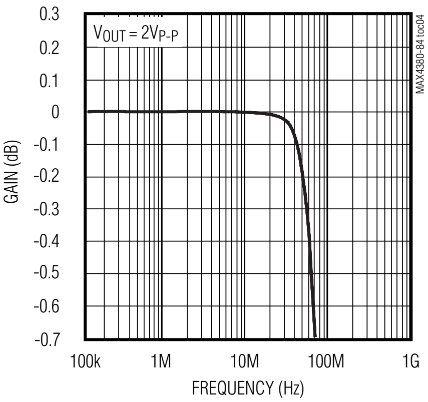




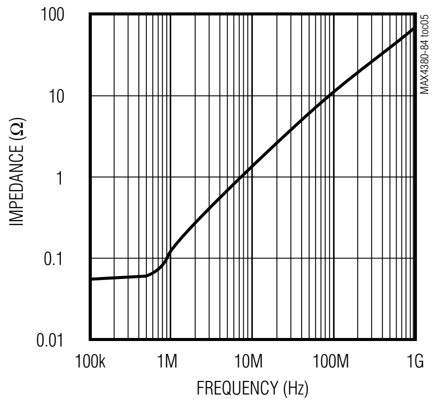
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, A_{VCL} = +1, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

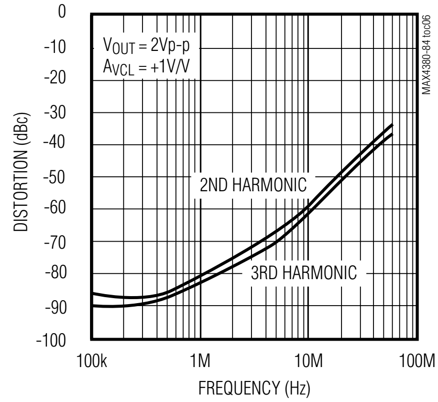
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



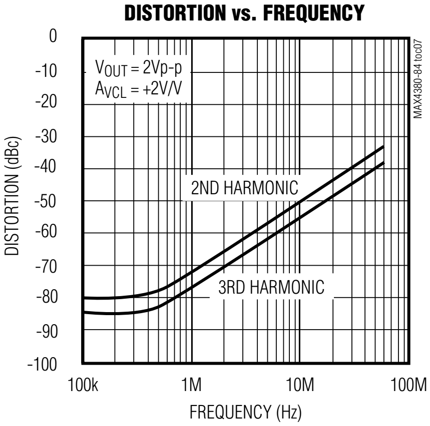
OUTPUT IMPEDANCE vs. FREQUENCY



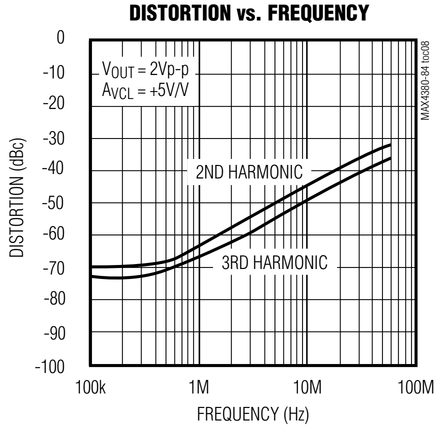
DISTORTION vs. FREQUENCY



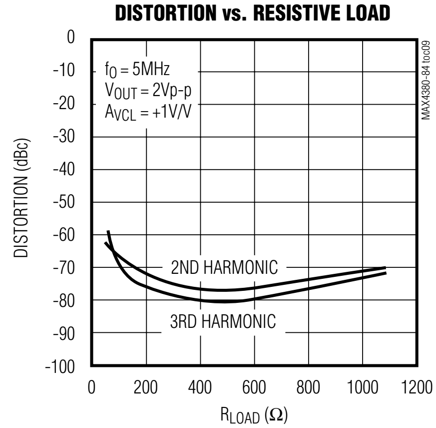
DISTORTION vs. FREQUENCY



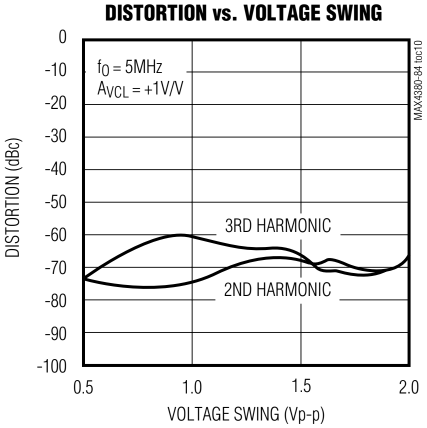
DISTORTION vs. FREQUENCY



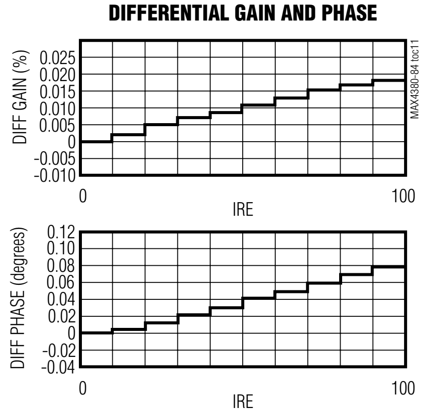
DISTORTION vs. RESISTIVE LOAD



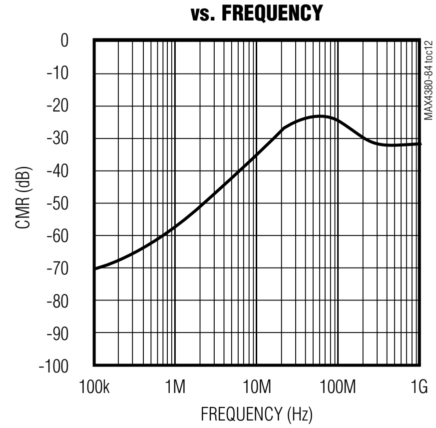
DISTORTION vs. VOLTAGE SWING



DIFFERENTIAL GAIN AND PHASE



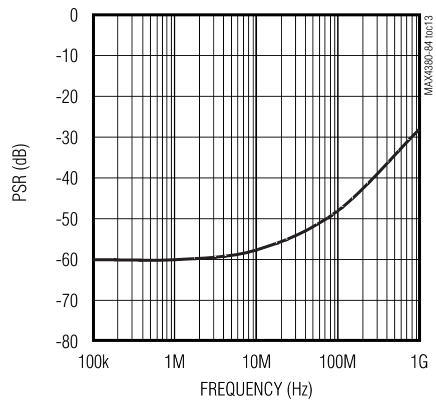
COMMON-MODE REJECTION vs. FREQUENCY



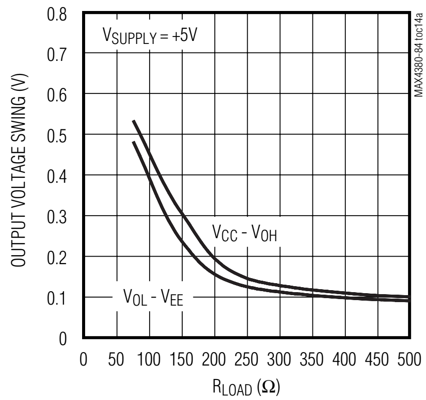
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, A_{VCL} = +1, R_L = 100Ω to $V_{CC}/2$, T_A = +25°C, unless otherwise noted.)

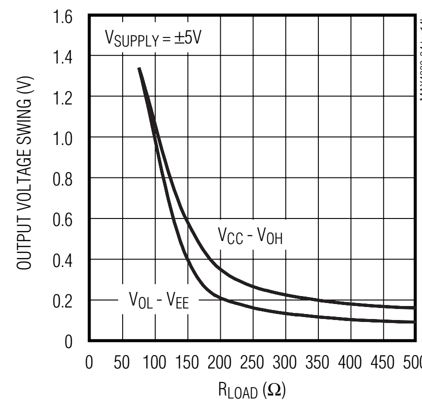
POWER-SUPPLY REJECTION vs. FREQUENCY



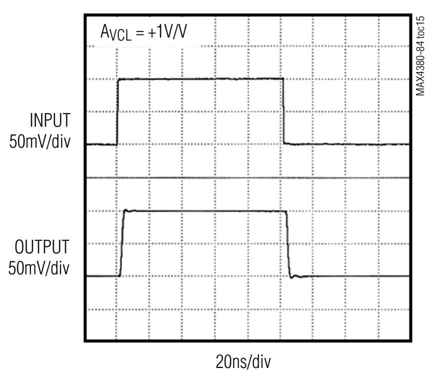
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



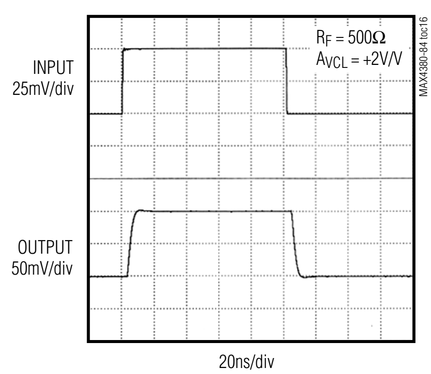
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



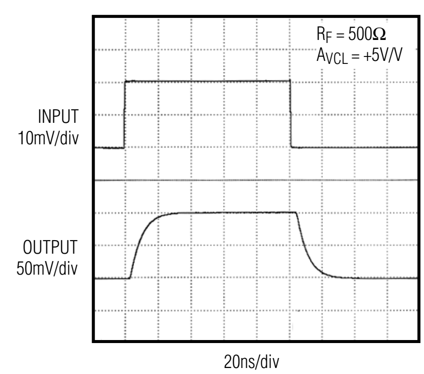
SMALL-SIGNAL PULSE RESPONSE



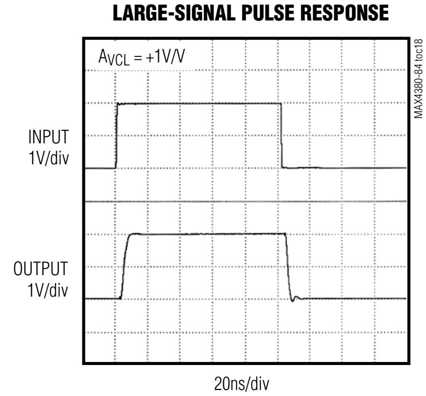
SMALL-SIGNAL PULSE RESPONSE



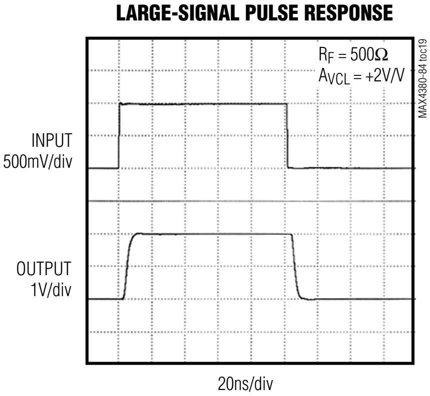
SMALL-SIGNAL PULSE RESPONSE



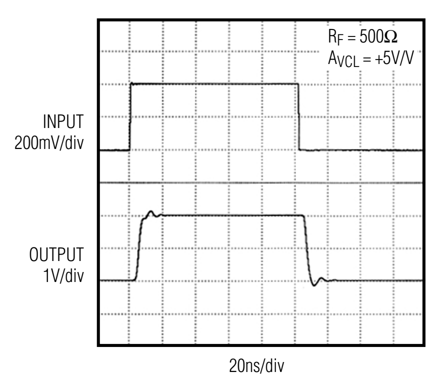
LARGE-SIGNAL PULSE RESPONSE



LARGE-SIGNAL PULSE RESPONSE



LARGE-SIGNAL PULSE RESPONSE

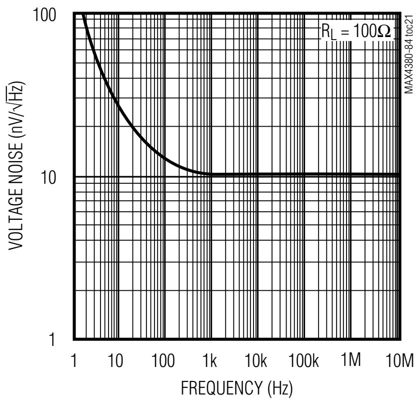


Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs and Disable

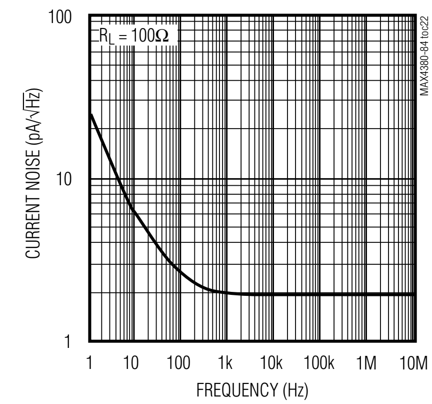
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, A_{VCL} = +1, R_L = 100Ω to $V_{CC}/2$, T_A = +25°C, unless otherwise noted.)

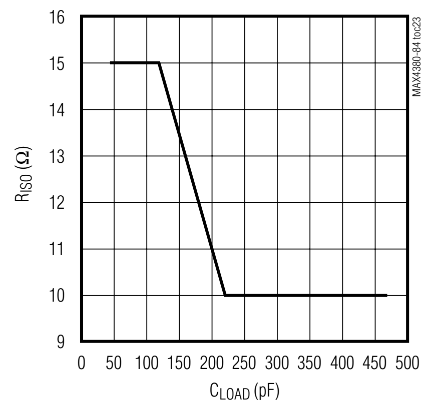
VOLTAGE NOISE vs. FREQUENCY



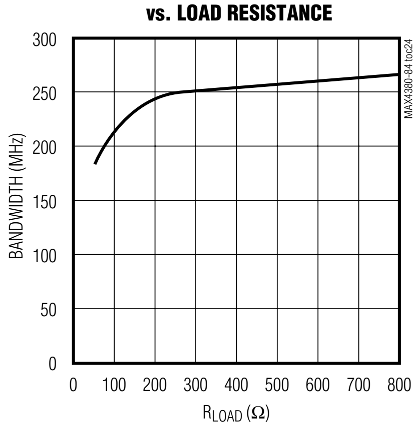
CURRENT NOISE vs. FREQUENCY



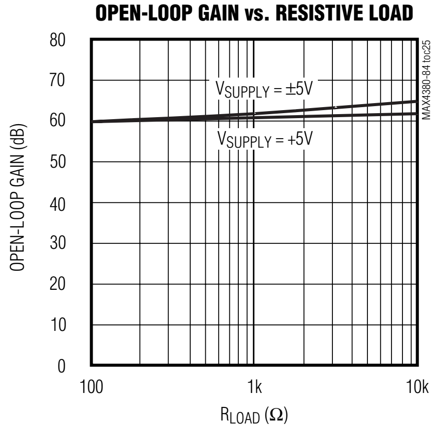
ISOLATION RESISTANCE vs. CAPACITIVE LOAD



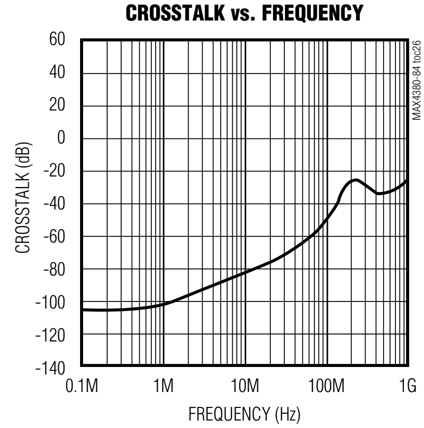
SMALL-SIGNAL BANDWIDTH vs. LOAD RESISTANCE



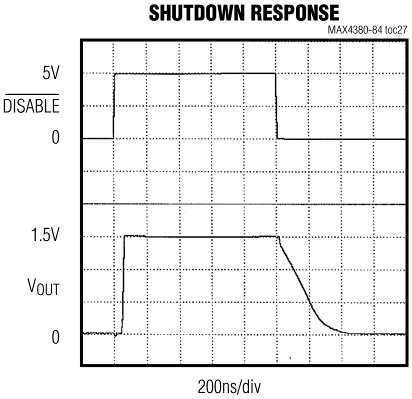
OPEN-LOOP GAIN vs. RESISTIVE LOAD



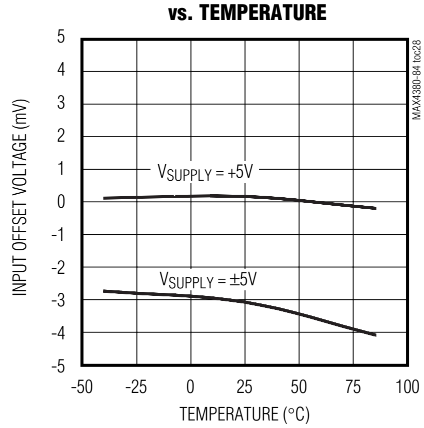
CROSSTALK vs. FREQUENCY



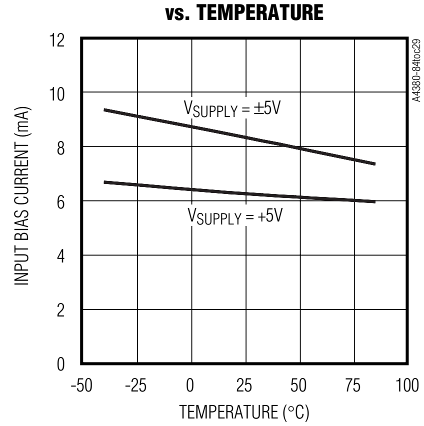
SHUTDOWN RESPONSE



INPUT OFFSET VOLTAGE vs. TEMPERATURE

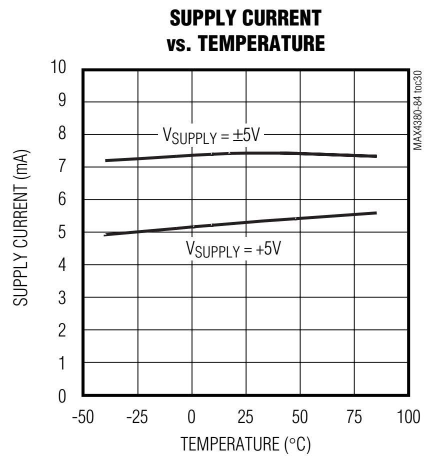


INPUT BIAS CURRENT vs. TEMPERATURE



Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +1.5V, A_{VCL} = +1, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN							NAME	FUNCTION
MAX4380	MAX4381	MAX4382		MAX4383		MAX4384		
SC70/SOT23	µMAX	QSOP	SO/TSSOP	SO/TSSOP	SO/QSOP	TSSOP		
6	10	4	4	4	4	5	V_{CC}	Positive Power Supply. Connect a 0.1µF capacitor to GND.
2	4	13	11	11	13	16	V_{EE}	Negative Power Supply. Connect a 0.1µF Capacitor to GND.
3	—	—	—	—	—	—	IN+	Noninverting Input
4	—	—	—	—	—	—	IN-	Inverting Input
1	—	—	—	—	—	—	OUT	Amplifier Output
5	—	—	—	—	—	—	$\overline{\text{DISABLE}}$	Disable. Connect to V_{CC} to Enable.
—	3	5	5	3	3	4	INA+	Amplifier A Noninverting Input
—	2	6	6	2	2	3	INA-	Amplifier A Inverting Input
—	1	7	7	1	1	2	OUTA	Amplifier A Output
—	5	1	1	—	—	1	$\overline{\text{DISABLEA}}$	Shutdown Amplifier A. Connect to V_{CC} to Enable.
—	7	12	10	5	5	6	INB+	Amplifier B Noninverting Input

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs and Disable

Pin Description (continued)

PIN							NAME	FUNCTION
MAX4380	MAX4381	MAX4382		MAX4383		MAX4384		
SC70/SOT23	µMAX	QSOP	SO/TSSOP	SO/TSSOP	SO/QSOP	TSSOP		
—	8	11	9	6	6	7	INB-	Amplifier B Inverting Input
—	9	10	8	7	7	8	OUTB	Amplifier B Output
—	6	3	3	—	—	9	$\overline{\text{DISABLEB}}$	Shutdown Amplifier B. Connect to V_{CC} to Enable.
—	—	14	12	10	12	15	INC+	Amplifier C Noninverting Input
—	—	15	13	9	11	14	INC-	Amplifier C Inverting Input
—	—	16	14	8	10	13	OUTC	Amplifier C Output
—	—	2	2	—	—	12	$\overline{\text{DISABLEC}}$	Shutdown Amplifier C. Connect to V_{CC} to Enable.
—	—	—	—	12	14	17	IND+	Amplifier D Noninverting Input
—	—	—	—	13	15	18	IND-	Amplifier D Inverting Input
—	—	—	—	14	16	19	OUTD	Amplifier D Output
—	—	—	—	—	—	20	$\overline{\text{DISABLED}}$	Shutdown Amplifier D. Connect to V_{CC} to Enable.
—	—	8, 9	—	—	8, 9	10, 11	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX4380–MAX4384 are single-supply, rail-to-rail, voltage-feedback amplifiers that employ current-feedback techniques to achieve 485V/µs slew rates and 210MHz bandwidths. Excellent harmonic distortion and differential gain/phase performance make these amplifiers an ideal choice for a wide variety of video and RF signal-processing applications.

Applications Information

The output voltage swings to within 50mV of each supply rail. Local feedback around the output stage ensures low open-loop output impedance to reduce gain sensitivity to load variations. The input stage permits common-mode voltages beyond the negative supply and to within 2.25V of the positive supply rail.

Choosing Resistor Values

Unity-Gain Configuration

The MAX4380–MAX4384 are internally compensated for unity gain. When configured for unity gain, a 24Ω resistor (R_F) in series with the feedback path optimizes AC performance. This resistor improves AC response by reducing the Q of the parallel LC circuit formed by the parasitic feedback capacitance and inductance.

Video Line Driver

The MAX4380–MAX4384 are low-power, voltage-feedback amplifiers featuring bandwidths up to 210MHz, 0.1dB gain flatness to 55MHz. They are designed to minimize differential-gain error and differential-phase error to 0.02% and 0.08 degrees respectively. They

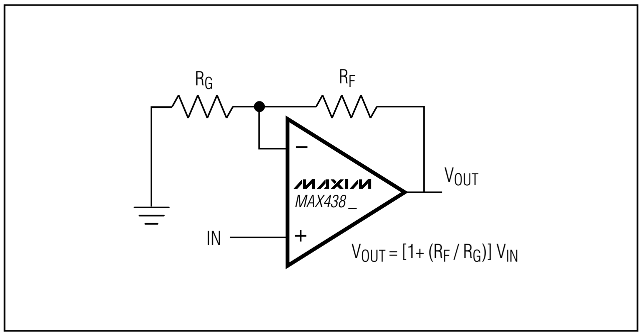


Figure 1a. Noninverting Gain Configuration

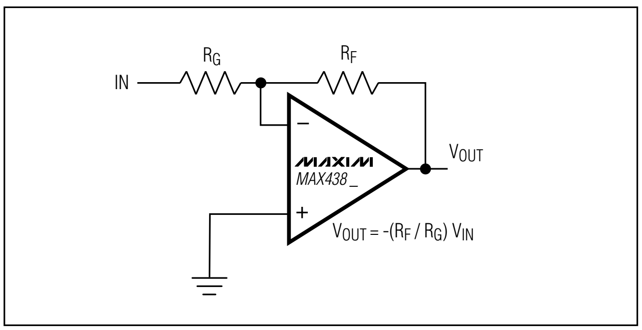


Figure 1b. Inverting Gain Configuration

have a 16ns settling time to 0.1%, 485V/µs slew rates, and output-current-drive capability of up to 75mA making them ideal for driving video loads.

Inverting and Noninverting Configurations

Select the gain-setting feedback (R_F) and input (R_G) resistor values to fit your application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros and decrease bandwidth or cause oscillations. For example, a noninverting gain-of-two configuration ($R_F = R_G$) using 1kΩ resistors, combined with 1pF of amplifier input capacitance and 1pF of PC board capacitance, causes a pole at 159MHz. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing the 1kΩ resistors to 100Ω extends the pole frequency to 1.59GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load resistor (Figures 1a and 1b).

Layout and Power-Supply Bypassing

These amplifiers operate from a single +4.5V to +11V power supply or from dual ±2.25V to ±5.5V supplies. For single-supply operation, bypass V_{CC} to ground with a 0.1µF capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1µF capacitor.

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the amplifier's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following design guidelines:

- Don't use wire-wrap boards; they are too inductive.
- Don't use IC sockets; they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Rail-to-Rail Outputs, Ground-Sensing Inputs

For +5V single-supply operation, the input common-mode range extends from (V_{EE} - 200mV) to (V_{CC} - 2.25V) with excellent common-mode rejection. Beyond this range, the amplifier output is a nonlinear function of the input, but does not undergo phase reversal or latchup.

For ±5V dual-supply operation, the common-mode range is from V_{EE} to (V_{CC} - 2.25V)

For +5V single-supply operation the output swings to within 50mV of either power-supply rail with a 2kΩ load. The input ground sensing and the rail-to-rail output substantially increase the dynamic range. With a symmetric input in a single +5V application, the input can swing 2.95Vp-p and the output can swing 4.9Vp-p with minimal distortion.

Low-Power Disable Mode

The disable feature ($\overline{\text{DISABLE\_}}$) allows the amplifier to be placed in a low-power, high-output-impedance state. When the disable pin ($\overline{\text{DISABLE\_}}$) is active, the amplifier's output impedance is 35kΩ. This high resistance and the low 2pF output capacitance make the MAX4380–MAX4382 and the MAX4384 ideal in RF/video multiplexer or switch applications. For larger arrays, pay careful attention to capacitive loading. Refer to the *Output Capacitive Loading and Stability* section.

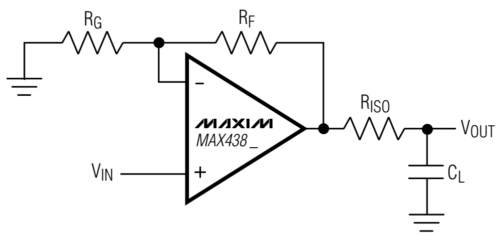


Figure 2. Driving a Capacitive Load Through an Isolation Resistor

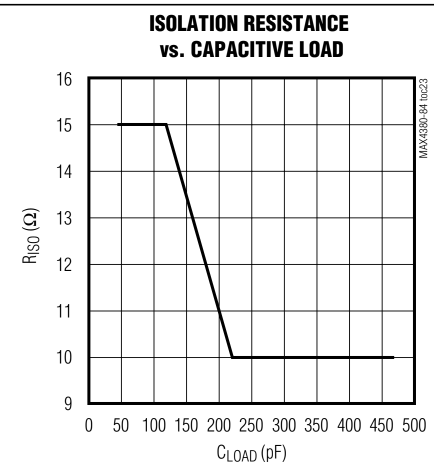


Figure 3. Isolation Resistance vs. Capacitive Load

Output Capacitive Loading and Stability

The MAX4380–MAX4384 are optimized for AC performance. They are not designed to drive highly reactive loads, which decrease phase margin and may produce excessive ringing and oscillation. Figure 2 shows a circuit that eliminates this problem. Figure 3 is a graph of the Optimal Isolation Resistor (R_S) vs. Capacitive Load. Figure 4 shows how a capacitive load causes excessive peaking of the amplifier's frequency response if the capacitor is not isolated from the amplifier by a resistor. A small isolation resistor (usually 10Ω to 15Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and the isolation resistor. Figure 5 shows the effect of a 15Ω isolation resistor on closed-loop response.

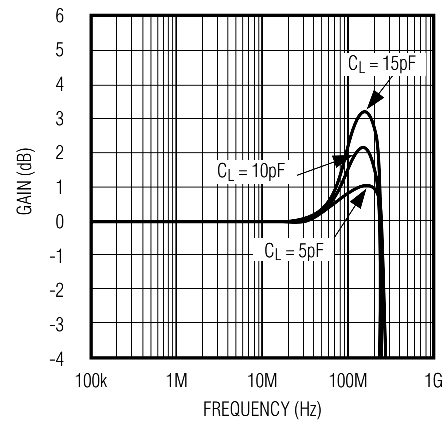


Figure 4. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

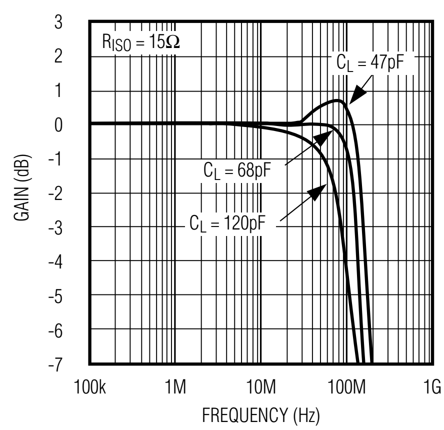


Figure 5. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Chip Information

MAX4380 TRANSISTOR COUNT: 66

MAX4381 TRANSISTOR COUNT: 132

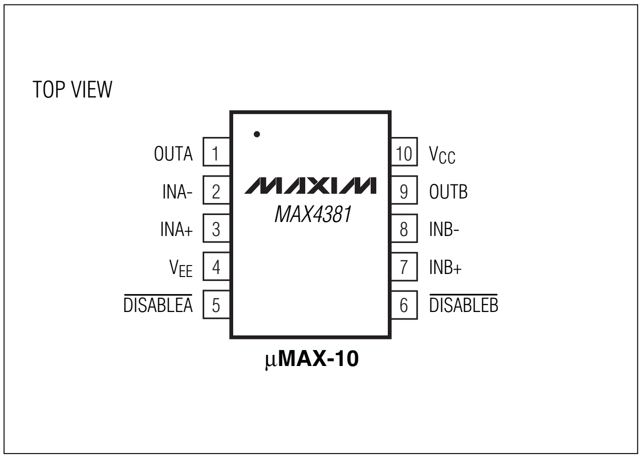
MAX4382 TRANSISTOR COUNT: 196

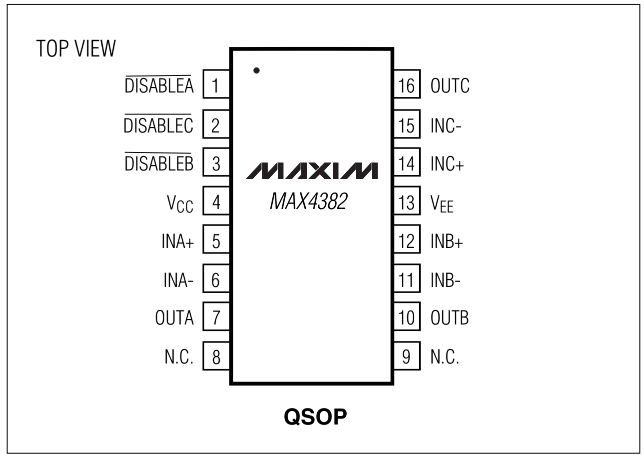
MAX4383 TRANSISTOR COUNT: 264

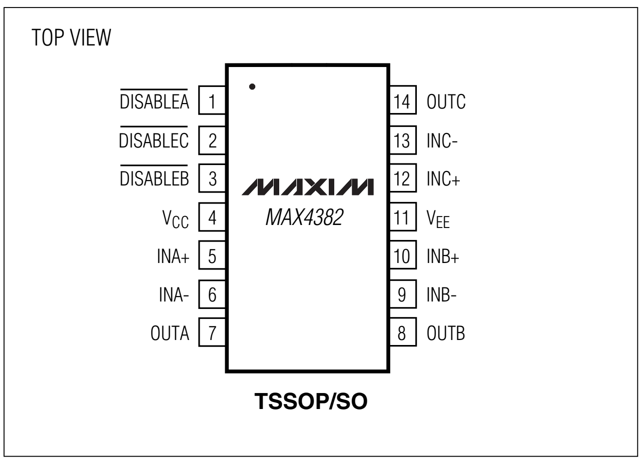
MAX4384 TRANSISTOR COUNT: 264

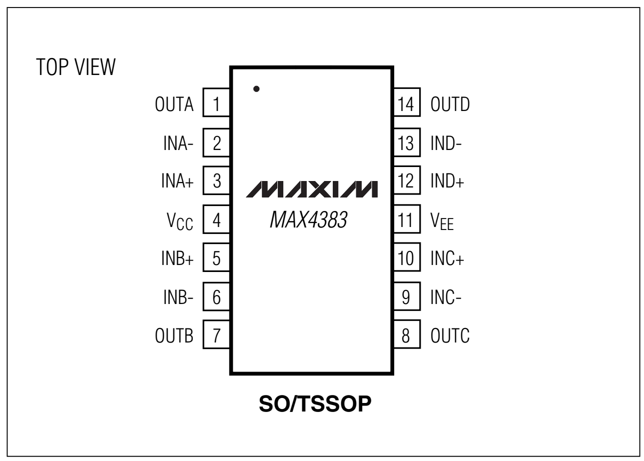
Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs and Disable

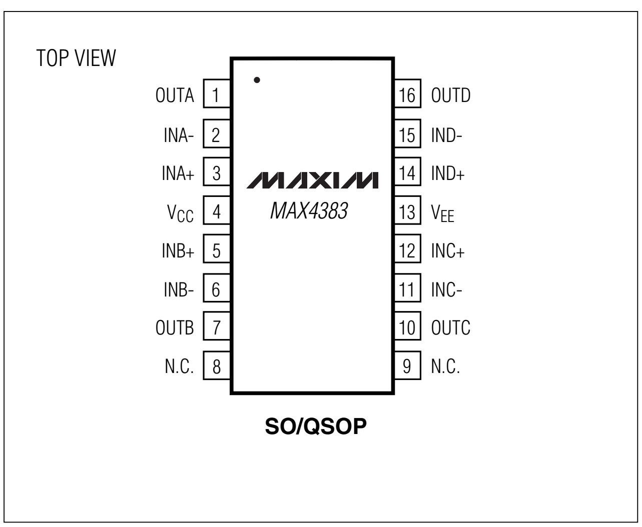
Pin Configurations (continued)

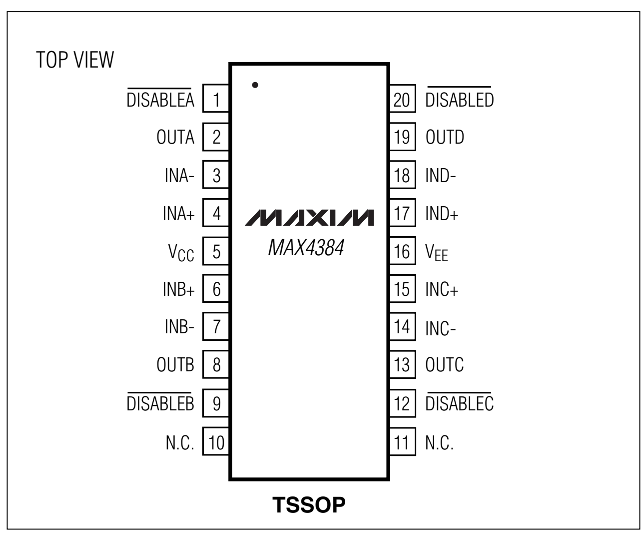








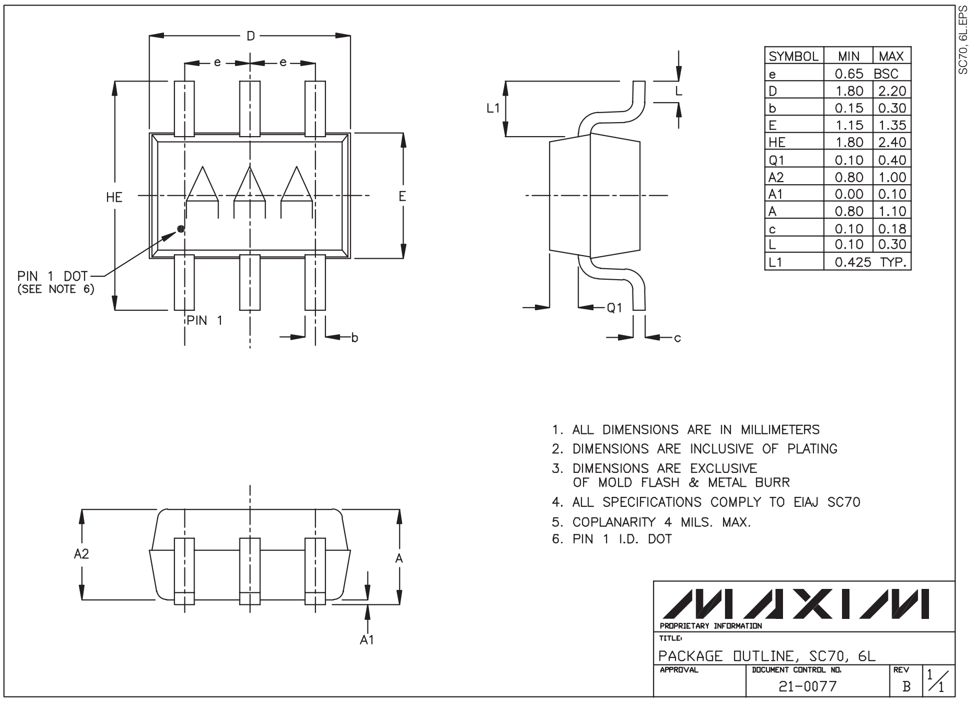


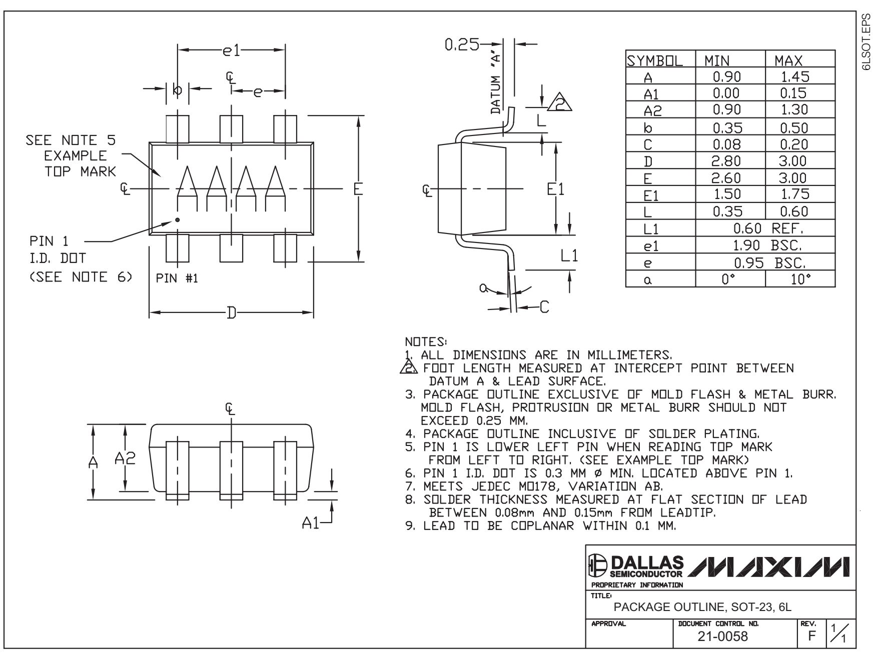


Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs and Disable

Package Information

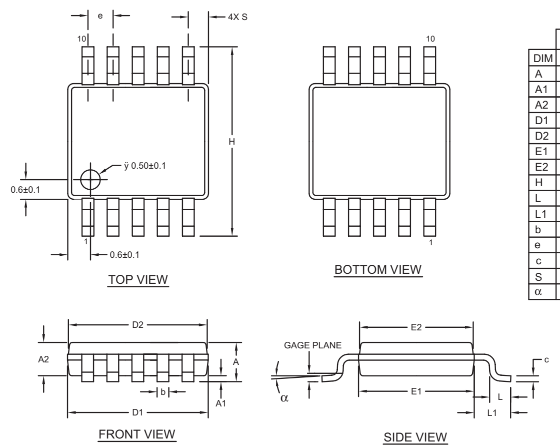
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)





Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

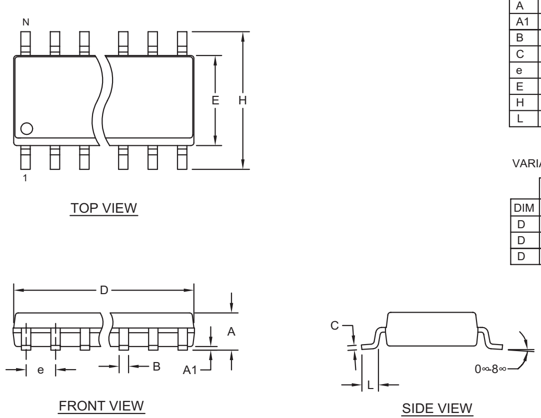


10LUMAX.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L uMAX/uSOP
APPROVAL | DOCUMENT CONTROL NO. 21-0061 | REV. I | 1/1



SOICN .EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

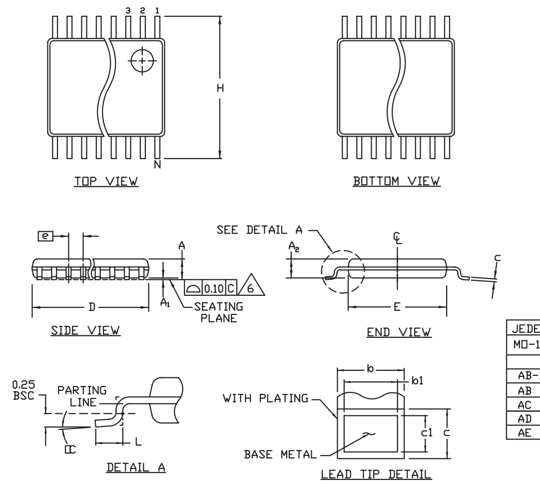
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, .150" SOIC
APPROVAL | DOCUMENT CONTROL NO. 21-0041 | REV. B | 1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



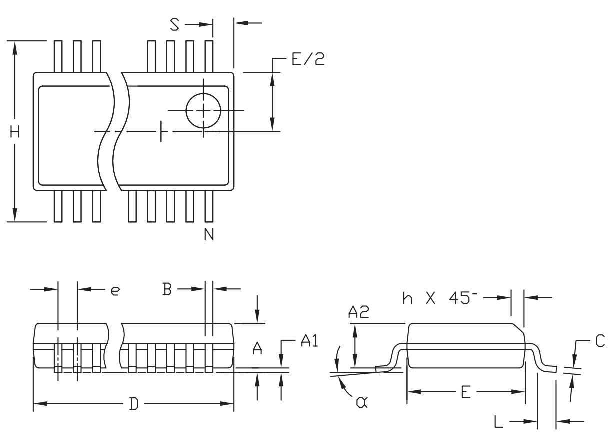
SYMBOL	COMMON DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC MO-153	N		VARIATIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV D | 1/1

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