Product/Process Change Notice - PCN 10_0262 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Material Report). Any issues with this PCN or requirements to qualify the change (additional data or samples) must be sent to ADI within 30 days of publication date. ADI contact information is listed below.

PCN Title: AD9547 mask change

Publication Date: 20-Oct-2010

Effectivity Date: 11-Nov-2010 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

1) The default value of a register bit has been changed instructing the Time to Digital Converter (TDC) to perform a single calibration per reference event, and simply remain in reset for the remainder of the inter-reference period.

2)Correct power connect to 1.8V PMOS device.

3)EEPROM controller circuit was redesigned similar to AD9557.

4)Changed Power on Reset (POR) circuit to assert reset as soon as the 1.8V supply is applied to the digital core. POR is released after multiple supplies are above 80% nominal threshold

5)Updated Die id to reflect new revision code

6)Remove auto-clear logic in the sync distribution register.

7)Soft I/O UPDATE fixed so it only triggers when the LSB of register 0x0005 is set (1).

8)The truncated bits LSBs from the beta and gamma multipliers are tracked digitally enabling adjustments to ensure the steady-state solution requires that the phases to be matched.

9)IRQ generation circuitry was altered so that an IRQ cannot be generated without being able to see (in status read-back) what generated it.

10)Added 50pF bypass capacitance to VREG, and adding series resistance between charge pump and loop filter (~250 ohms), and between loop filter and VCO tune input (~150 ohms). This results in better phase noise performance for many configurations.

11)Each profile has a new bit “Phase Lock Scale” in the first register byte (MSB bit) – see register map version (3.0.0 or later). This selects a scale for the phase lock threshold of nanoseconds (default is picoseconds).

Reason For Change

1) This enables the device to work well with very jittery reference.

2) Improve long term operation.

3) In order to reload the EEPROM following a chip reset, the user would have to perform a reset without loading the EEPROM first. This enables the EEPROM to work as originally specified.

4) EEPROM intermittently corrupted at power on reset. Supply sequencing may cause improper part initialization. This enables the EEPROM to work as specified.

5) Die ID indicates new revision.

6) Sync distribution register also calibrates system clock edge. User was unable to synchronize distribution with software control bit without also calibrating the system clock. This enables the sync function to work as originally intended.

7) I2C soft I/O UPDATE is triggering when it shouldn’t. In the old die, I/O UPDATE triggers whether this bit is 0 or 1. This enables the Soft I/O Update to work as specified

8) Loop Filter data precision error. Truncation of LSBs in beta and gamma multipliers causes loop instability for small phase errors. The incorrect

loop response allows any phase which results in no change in the average frequency to be a steady-state solution, meaning that one or more non-zero phase difference might be misread as steady-state. This enables the device to function properly, as specified

9) If an IRQ capable event, such as "system clock calibration started", occurs prior to the relevant bit in the selection mask being set, the IRQ pin will be asserted, but the status register will not indicate which event happened. The IRQ can only be cleared by clearing the specific event register, a global "clear all IRQs" is not sufficient. This enables the IRQ function to work as specified

10)LCVCO Jitter exhibited undesirable peaking issues. This improves the noise performance of the device

11)MAX Phase detector threshold range was lower than desired. The threshold is limited to 16-bits, so 2^16 picoseconds is 65.5 ns, whereas 2^16 nanoseconds is 65.5 us. For applications like GPS or IEEE1588, reference jitter may be larger than 65.5 ns, and the device needs to function properly even with this level of jitter. An extended scale for the threshold allows high jitter references to be more easily accommodated. This enables the device to work with very jittery reference inputs as originally intended

Impact of the change (positive or negative) on fit, form, function & reliability

None to the fit or form. Long term operation is improved. Functionality to datasheet is corrected.

Product Identification *(this section will describe how to identify the changed material)*

New material will all have date codes of 1040 or greater.

Summary of Supporting Information

See attached qual plan summary.

Supporting Documents

Attachment 1: Type: Qualification Plan Summary

ADI_PCN_10_0262_Rev_-_AD9548.doc

For questions on this PCN, send email to the regional contacts below or contact your local ADI sales representative					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models	
Added Parts On This Revision - Product Family / Model Number (2)	
AD9547 / AD9547BCPZ	AD9547 / AD9547BCPZ-REEL7

Appendix B - Revision History		
Rev	**Publish Date**	**Rev Description**
Rev. -	20-Oct-2010	Initial Release