Keywords: E1 transceivers, single chip tranceiver, SCT, 4 port, signaling, G.703, quad E1, transceiver

APPLICATION NOTE 395

DS21Q59 vs. DS21Q50 Quad E1 Transceivers

Sep 10, 2002

Abstract: Application note 395 is provided for users of the DS21Q50 quad E1 transceiver whose application requires transmit and receive signaling. The DS21Q59 is pin-to-pin compatible and contains all the features of the DS21Q50 while adding signaling support. The DS21Q59 can be used in an existing DS21Q50 application without hardware or software modification.

Overview

This document is provided for users of the DS21Q50 quad E1 transceiver whose application requires transmit and receive signaling. The DS21Q59 is pin-to-pin compatible and contains all the features of the DS21Q50 while adding signaling support. The DS21Q59 can be used in an existing DS21Q50 application without hardware or software modification. The DS21Q59 data sheet provides a complete description of all the functionality of the DS21Q59. All differences between the DS21Q59 and DS21Q50 are presented in the order of appearance in the DS21Q59 data sheet. This allows current DS21Q50 users to focus on the required information for using the DS21Q59.

Register Map

The DS21Q50 contains five common control registers and three test registers. The DS21Q59 contains two additional common control registers for a total of seven and only one test register. Table 1 highlights the differences in the register maps of each device.

Table 1. Register Map

Address	DS21Q50	DS21Q59
Range	00h–2Fh	00h–3Fh
1Eh	Test 2	Test 2
1Fh	Test 3	CCR7
2Fh	Test1	CCR6
30h–3Fh	Unused	Signaling Access Registers

DS21Q59 Common Control Register Functionality

Common Control Register (16h) CCR5.5

Line Interface G.703 Synchronization Interface Enable bit (CCR5.5 LIUSI)
DS21Q50: Enables both the receiver and transmitter at the same time.
DS21Q59: Works in conjunction with CCR7.0 to select G.703 functionality on receiver and transmitter.

Table 2 shows the G.703 Synchronization Interface function of the DS21Q59.

Table 2. G.703 Function

LIUSI (CCR5.5)	TG703 (CCR7.0)	Function
0	0	Transmit and receive function normally
0	1	Transmit G.703 signal, receiver functions normally
1	0	Transmit and receive G.703 signal
1	1	Receive G.703, transmitter functions normally

Common Control Register 6 (2Fh)

Symbol	BIT	Name and Description
OTM1	7	**Output Test Mode 1** (Table 3)
OTM1	6	**Output Test Mode 0** (Table 3)
SRAS	5	**Signaling Read Access Select.** This bit controls the function of registers SA1 through SA16 when reading. 0 = Reading SA1—SA16 accesses receive signaling data 1 = Reading SA1—SA16 accesses transmit signaling data
LTC/SC	4	**Loss-of-Transmit Clock/Signaling Change-of-State Select.** This bit determines how the status register bit at SR2.2 operates. 0 = SR2.2 indicates loss-of-transmit clock 1 = SR2.2 indicates signaling data has changed states since the last multiframe
T16S	3	**Time Slot 16 Select.** Transmit signaling insertion enable. 0 = signaling is not inserted into the transmit path from SA1—SA16 1 = signaling is inserted into the transmit path from SA1—SA16
—	2	**Unused.** Should be set = 0 for proper operation
—	1	**Unused.** Should be set = 0 for proper operation
RESET	0	**RESET.** A low-to-high transition of this bit resets all register bits to 0.

For normal CAS operation, set CCR6.5 = 0, CCR6.4 = 1, CCR6.3 = 1.

Table 3. Output Modes

OTM1	OTM0	Outputs
0	0	Normal Operation
0	1	Outputs in Tri-state
1	0	Outputs Low
1	1	Outputs High

Common Control Register 7 (1Fh)

Symbol	BIT	NAme and Description
—	7	**Unused.** Should be set = 0 for proper operation
—	6	**Unused.** Should be set = 0 for proper operation
—	5	**Unused.** Should be set = 0 for proper operation
—	4	**Unused.** Should be set = 0 for proper operation
136S	3	**1:1.36 Transformer Select** 0 = 1:2 transmit transformer 1 = 1:1.36 or 1:1.6 transmit transformer (Table 4)
ALB	2	**Analog Loopback.** Setting this bit internally connects TTIP and TRING to RTIP and RRING. The external signal at the RTIP and RRING pins is ignored.
—	1	**Unused.** Should be set = 0 for proper operation
TG703	0	**Transmit G.703.** This control bit works in conjunction with CCR5.5 to select G.703 functionality on the transmitter and receiver (Table 7.2 of data sheet). These bits determine whether the line receiver and transmitter should receive/transmit a normal E1 signal (Section 6 of G.703) or a 2.048MHz synchronization signal (Section 10 of G.703).

Table 4. Transformer Select CCR7.3 (136S)

136S	L2	L1	L0	Application	Transformer1:1.6	Transformer1:1.36
1	0	0	0	75Ω	Rt=0Ω	NM
1	0	0	1	120Ω	Rt=0Ω	NM
1	0	1	0	75Ω	Rt=2.7Ω	Rt=0O
1	0	1	1	120Ω	Rt=3.3Ω	Rt=0O
1	1	0	0	NM	NM	NM
1	1	0	1	NM	NM	NM
1	1	1	0	NM	NM	NM
1	1	1	1	NM	NM	NM

NM=Not Meaningful

Status and Information Registers

Interrupt Handling

DS21Q50: Each port must be polled to determine the source of the interrupt.
DS21Q59: By reading one of the unused addresses on any port (0Ch, 0Dh, 0Eh) the user can determine which status register in the four ports is causing the interrupt. The following table shows the contents of any of the unused registers.

Address (0Ch,0Dh,0Eh) of any port

Symbol	BIT	NAme and Description
SR2P4	7	**Status Register 2 Port 4.** A 1 in this bit position indicates that status register 2 in port 4 is asserting an interrupt.
SR1P4	6	**Status Register 1 Port 4.** A 1 in this bit position indicates that status register 1 in port 4 is asserting an interrupt.
SR2P3	5	**Status Register 2 Port 3.** A 1 in this bit position indicates that status register 2 in port 3 is asserting an interrupt.
SR1P3	4	**Status Register 1 Port 3.** A 1 in this bit position indicates that status register 1 in port 3 is asserting an interrupt.
SR2P2	3	**Status Register 2 Port 2.** A 1 in this bit position indicates that status register 2 in port 2 is asserting an interrupt.
SR1P2	2	**Status Register 1 Port 2.** A 1 in this bit position indicates that status register 1 in port 2 is asserting an interrupt.
SR2P1	7	**Status Register 2 Port 1.** A 1 in this bit position indicates that status register 2 in port 1 is asserting an interrupt.
SR1P1	7	**Status Register 1 Port 1.** A 1 in this bit position indicates that status register 1 in port 1 is asserting an interrupt.

Status Register 2 (0Bh) SR2.2

Symbol	BIT	NAme and Description
LOTC	2	**Loss-of-Transmit Clock** Function controlled by CCR6.4(LTC/SC) Indicates loss-of-transmit clock if CCR6.4 = 0 Indicates signaling data has changed states since the last multiframe if CCR6.4 = 1

Interrupt Mask Register 2 (19h) IMR2.2

Symbol	BIT	NAme and Description
LOTC	2	**Loss-of-Transmit Clock** Function controlled by CCR6.4(LTC/SC) Loss-of-transmit clock interrupt mask if CCR6.4 = 0 Signaling data changed interrupt mask if CCR6.4 = 1 0 = interrupt masked 1 = interrupt enabled

Signaling Operation

Registers SA1 to SA16 are used to access the transmit and receive signaling data. Normally, reading these registers accesses the receive signaling data and writing these registers sources signaling data for the transmitter. The user can read what was written to the transmit signaling buffer by setting CCR6.5 = 1, then reading SA1 to SA16. In most applications however, CCR6.5 should be set = 0.

Receive Signaling

Signaling data is sampled from time slot 16 in the receive data stream and copied into the receive

signaling buffers. The host can access the signaling data by reading SA1 through SA16. The signaling information in these registers is always updated on CAS multiframe boundaries. The SR2.7 bit in status register 2 can be used to alert the host that new signaling data is present in the receive signaling buffers. The host has 2ms to read the signaling buffers before they are updated. In common channel signaling mode (CCS), the SR2.7 bit in status register 2 is used to alert the host that new signaling data is present in the receive signaling buffers.

Transmit Signaling

Insertion of signaling data from the transmit signaling buffers is enabled by setting CCR6.3 = 1. Signaling data is loaded into the transmit-signaling buffers by writing the signaling data to SA1 to SA16. On multiframe boundaries, the contents of the transmit signaling buffer is loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can use the transmit multiframe interrupt in status register 2 (SR2.5) to know when to update the signaling bits. The host has 2ms to update the signaling data. The user only needs to update the signaling data that has changed since the last update.

Cas Operation

For CAS mode, the user must provide the CAS alignment pattern (four 0s in the upper nibble of TS16). Typically this is done by setting the upper 4 bits of SA1 = 0. The lower four bits are alarm bits. The user only needs to update the appropriate channel associated signaling data in SA2 to SA16 on multiframe boundaries.

SA1 to SA16–Signaling Registers (30h–3Fh)

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	SA1
CH1-A	CH1-B	CH1-C	CH1-D	CH16-A	CH16-B	CH16-C	CH16-D	SA2
CH2-A	CH2-B	CH2-C	CH2-D	CH17-A	CH17-B	CH17-C	CH17-D	SA3
CH3-A	CH3-B	CH3-C	CH3-D	CH18-A	CH18-B	CH18-C	CH18-D	SA4
CH4-A	CH4-B	CH4-C	CH4-D	CH19-A	CH19-B	CH19-C	CH19-D	SA5
CH5-A	CH5-B	CH5-C	CH5-D	CH20-A	CH20-B	CH20-C	CH20-D	SA6
CH6-A	CH-6B	CH-6C	CH-6D	CH-21-A	CH21-B	CH21-C	CH21-D	SA7
CH7-A	CH7-B	CH7-C	CH7-D	CH22-A	CH22-B	CH22-C	CH22-D	SA8
CH8-A	CH8-B	CH8-C	CH8-D	CH23-A	CH23-B	CH23-C	CH23-D	SA9
CH9-A	CH9-B	CH9-C	CH9-D	CH24-A	CH24-B	CH24-C	CH24-D	SA10
CH10-A	CH10-B	CH10-C	CH10-D	CH25-A	CH25-B	CH25-C	CH25-D	SA11
CH11-A	CH11-B	CH11-C	CH11-D	CH26-A	CH26-B	CH26-C	CH26-D	SA12
CH12-A	CH12-B	CH12-C	CH12-D	CH27-A	CH27-B	CH27-C	CH27-D	SA13
CH13-A	CH13-B	CH13-C	CH13-D	CH28-A	CH28-B	CH28-C	CH28-D	SA14
CH14-A	CH14-B	CH14-C	CH14-D	CH29-A	CH29-B	CH29-C	CH29-D	SA15
CH15-A	CH15-B	CH15-C	CH15-D	CH30-A	CH30-B	CH30-C	CH30-D	SA16

Related Parts	
DS21Q50	Quad E1 Transceiver
DS21Q59	E1 Quad Transceiver

More Information
For Technical Support: http://www.maximintegrated.com/support
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APPLICATION NOTE 395, AN395, AN 395, APP395, Appnote395, Appnote 395