

# Low-Voltage SPDT Analog Switch or 2:1 Multiplexer/ De-multiplexer Bus Switch

## NC7SBU3157, FSAU3157

### General Description

The NC7SBU3157 / FSAU3157 is a high-performance, single-pole / double-throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5 V  $V_{CC}$  operating range. The control input tolerates voltages up to 5.5V, independent of the  $V_{CC}$  operating range.

ON Semiconductor integrated Undershoot Hardened Circuit senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning the switch on.

### Features

- Analog and Digital Applications
- Space-saving, SC70 6-lead, Surface-mount Package
- Low On Resistance:  $<10 \Omega$  on typical at 3.3 V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range: 1.65 V to 5.5 V
- Rail-to-rail Signal Handling
- Power-down, High-impedance Control Input
- Over-voltage Tolerance of Control Input to 7.0 V
- Break-before-make Enable Circuitry
- 250 MHz, 3 dB Bandwidth
- This Device is Pb-Free and is RoHS Compliant

### FUNCTION TABLE

Input (S)	Function
Logic Level Low	$B_0$ Connected to A
Logic Level High	$B_1$ Connected to A

### PIN DESCRIPTIONS

Pin Names	Description
A, $B_0$ , $B_1$	Data Ports
S	Control Input



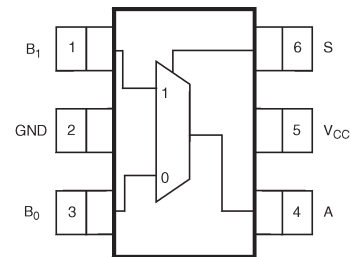
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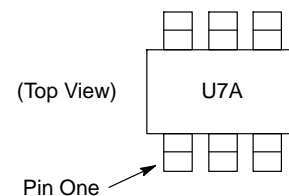
SC-88 (SC-70 6 Lead), 1.25x2  
CASE 419AD

### CONNECTION DIAGRAM



Pin Assignment SC-70

### MARKING DIAGRAM



#### NOTE:

Orientation of top mark determines pin one location. Read the top mark left to right and pin one is the lower left pin.

Pin One Orientation

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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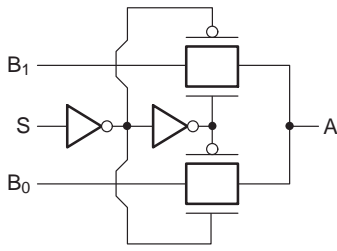


Figure 1. Logic Symbol

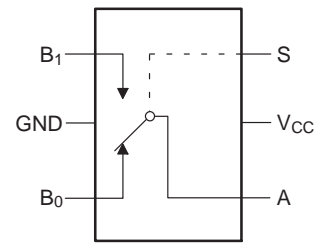


Figure 2. Analog Symbol

## ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature Range	Package	Shipping†
NC7SBU3157P6X	U7A	-40 to 85°C	SC70 (Pb-Free)	3000 units / Tape & Reel
FSAU3157P6X	U7A	-40 to 85°C	SC70 (Pb-Free)	3000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	-0.5	+7.0	V
$V_S$	DC Switch Voltage (Note 1)	-0.5	$V_{CC} + 0.5$	V
$V_{IN}$	DC Input Voltage (Note 1)	-0.5	+7.0	V
$I_{IK}$	DC Input Diode Current at $V_{IN} < 0$ V		-50	mA
$I_{OUT}$	DC Output Current		128	mA
$I_{CC}/I_{GND}$	DC $V_{CC}$ or Ground Current		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Junction Temperature Under Bias		+150	°C
$T_L$	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
$P_D$	Power Dissipation at +85°C		180	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units	
$V_{CC}$	Supply Voltage Operating	1.65	5.50	V	
$V_{IN}$	Control Input Voltage (Note 2)	0	$V_{CC}$	V	
$V_{IN}$	Switch Input Voltage (Note 2)	0	$V_{CC}$	V	
$V_{OUT}$	Output Voltage (Note 2)	0	$V_{CC}$	V	
$T_A$	Operating Temperature	-40	+85	°C	
$t_r, t_f$	Input Rise and Fall Time	Control Input $V_{CC} = 2.3$ V – 3.6 V	0	10	ns/V
		Control Input $V_{CC} = 4.5$ V – 5.5 V	0	5	ns/V
$\theta_{JA}$	Thermal Resistance		350	°C/W	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Control input must be held HIGH or LOW; it must not float.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage		1.65 to 1.95	0.75 V <sub>CC</sub>			0.75 V <sub>CC</sub>		V
			2.3 to 5.5	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		
V <sub>IL</sub>	Low Level Input Voltage		1.65 to 1.95			0.25 V <sub>CC</sub>		0.25 V <sub>CC</sub>	V
			2.3 to 5.5			0.3 V <sub>CC</sub>		0.3 V <sub>CC</sub>	
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5V	0 to 5.5		±0.05	±0.1		±1	μA
I <sub>OFF</sub>	Off State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	1.65 to 5.5		±0.05	±0.1		±1	μA
R <sub>ON</sub>	Switch On Resistance (Note 3)	V <sub>IN</sub> =0V, I <sub>O</sub> =30mA	4.5		3.0	15.0		15.0	Ω
		V <sub>IN</sub> =2.4V, I <sub>O</sub> =-30mA			5.0	15.0		15.0	
		V <sub>IN</sub> =4.5V, I <sub>O</sub> =-30mA			7.0	15.0		15.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =24mA	3.0		4.0	20.0		20.0	
		V <sub>IN</sub> =3V, I <sub>O</sub> =-24mA			10.0	20.0		20.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =8mA	2.3		5.0	30.0		30.0	
		V <sub>IN</sub> =2.3V, I <sub>O</sub> =-8mA			13.0	30.0		30.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =4mA	1.65		6.5	50.0		50.0	
V <sub>IN</sub> =1.65V, I <sub>O</sub> =-4mA		17.0		50.0		50.0			
I <sub>CC</sub>	Quiescent Supply Current; All Channels On or Off	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0	5.5			1		10	μA
	Analog Signal Range		V <sub>CC</sub>	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V
R <sub>RANGE</sub>	On Resistance Over Signal Range (Notes 3, 7)	I <sub>A</sub> =-30mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	4.5					25.0	Ω
		I <sub>A</sub> =-24mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.0				50.0		
		I <sub>A</sub> =-8mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.3				100		
		I <sub>A</sub> =-4mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.65				300		
ΔR <sub>ON</sub>	On Resistance Match Between Channels (Notes 3, 4, 5)	I <sub>A</sub> =-30mA, V <sub>Bn</sub> =3.15	4.5		0.15				Ω
		I <sub>A</sub> =-24mA, V <sub>Bn</sub> =2.1	3.0		0.2				
		I <sub>A</sub> =-8mA, V <sub>Bn</sub> =1.6	2.3		0.5				
		I <sub>A</sub> =-4mA, V <sub>Bn</sub> =1.15	1.65		0.5				
V <sub>IKU</sub>	Voltage Under-shoot	0.0mA ≤ I <sub>IN</sub> ≤ -50, $\overline{OE}$ 5.5v	5.5					-2	V
R <sub>flat</sub>	On Resistance Flatness (Notes 3, 4, 6)	I <sub>A</sub> =-30mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	5.0		6.0				Ω
		I <sub>A</sub> =-24mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.3		12.0				
		I <sub>A</sub> =-8mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.5		28.0				
		I <sub>A</sub> =-4mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.8		125				

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized, but not tested in production.
5. ΔR<sub>ON</sub> = R<sub>ON</sub> max - R<sub>ON</sub> minimum measured at identical V<sub>CC</sub>, temperature, and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
7. Guaranteed by design.

**AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	VCC (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus-to-Bus (Note 8)	V <sub>I</sub> = OPEN	1.65 to 1.95						ns	Figure 5 Figure 6
			2.3 to 2.7			1.2		1.2		
			3.0 to 3.6			0.8		0.8		
			4.5 to 5.5			0.3		0.3		
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time Turn-On Time (A to B <sub>n</sub> )	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> = 0 V for t <sub>PZH</sub>	1.65 to 1.95	7.0		23.0	7.0	24.0	ns	Figure 5 Figure 6
			2.3 to 2.7	3.5		13.0	3.5	14.0		
			3.0 to 3.6	2.5		6.9	2.5	7.6		
			4.5 to 5.5	1.7		5.2	1.7	5.7		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time Turn-Off Time (A Port to B Port)	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> = 0 V for t <sub>PHZ</sub>	1.65 to 1.95	3.0		12.5	3.0	13.0	ns	Figure 5 Figure 6
			2.3 to 2.7	2.0		7.0	2.0	7.5		
			3.0 to 3.6	1.5		5.0	1.5	5.3		
			4.5 to 5.5	0.8		3.5	0.8	3.8		
t <sub>BBM</sub>	Break-Before-Make Time (Note 9)		1.65 to 1.95	0.5			0.5		ns	Figure 7
			2.3 to 2.7	0.5			0.5			
			3.0 to 3.6	0.5			0.5			
			4.5 to 5.5	0.5			0.5			
Q	Charge Injection (Note 9)	C <sub>L</sub> = 0.1 nF, V <sub>GEN</sub> = 0 V	5.0		7.0			pC	Figure 8	
		R <sub>GEN</sub> = 0 Ω	3.3		3.0					
OIRR	Off Isolation (Note 10)	R <sub>L</sub> = 50 Ω, f = 10 MHz	1.65 to 5.5		-57.0			dB	Figure 9	
Xtalk	Crosstalk	R <sub>L</sub> = 50 Ω, f = 10 MHz	1.65 to 5.5		-54.0			dB	Figure 10	
BW	-3dB Bandwidth	R <sub>L</sub> = 50 Ω	1.65 to 5.5		250			MHz	Figure 13	
THD	Total Harmonic Distortion (Note 9)	R <sub>L</sub> = 600 Ω, 0.5 V <sub>PP</sub> , f = 20 Hz to 20 KHz	5.0		.011			%		

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).  
 9. Guaranteed by design.  
 10. Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub> / V<sub>Bn</sub>].

**CAPACITANCE** (Note 11)

Symbol	Parameter	Conditions	Typ.	Max.	Units	Figure
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 0 V	2.3		pF	
C <sub>IO-B</sub>	B Port Off Capacitance	V <sub>CC</sub> = 5.0 V	6.5		pF	Figure 11
C <sub>IOA-ON</sub>	A Port Capacitance When Switch Is Enabled	V <sub>CC</sub> = 5.0 V	18.5		pF	Figure 12

11. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized, but not tested in production.

**UNDERSHOOT CHARACTERISTIC** (Note 12)

Symbol	Parameter	Min.	Typ.	Units	Figure
V <sub>OUTU</sub>	Output Voltage During Undershoot	2.5	V <sub>OH</sub> - 0.3	V	Figure 3

12. This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

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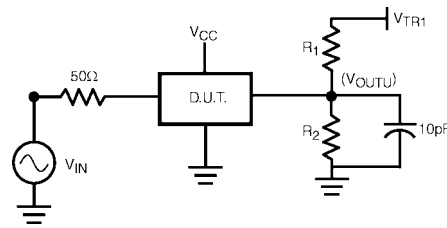


Figure 3. Output Voltage During Undershoot

## DEVICE TEST CONDITIONS

Parameter	Value	Units
$V_{IN}$	see Figure 4	V
$R_1 = R_2$	100	K $\Omega$
$V_{TRI}$	7.0	V
$V_{CC}$	5.5	V

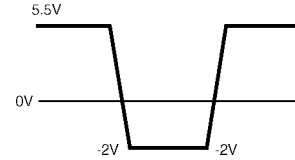
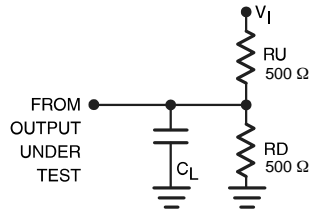


Figure 4. Transient Input Voltage Waveform

## AC Loading and Waveforms



### Notes:

Input driven by 50  $\Omega$  source terminated in 50  $\Omega$ .  
 $C_L$  includes load and stray capacitance,  $C_L = 50$  pF  
 Input PRR = 1.0 MHz,  $t_W = 500$  ns

Figure 5. AC Test Circuit

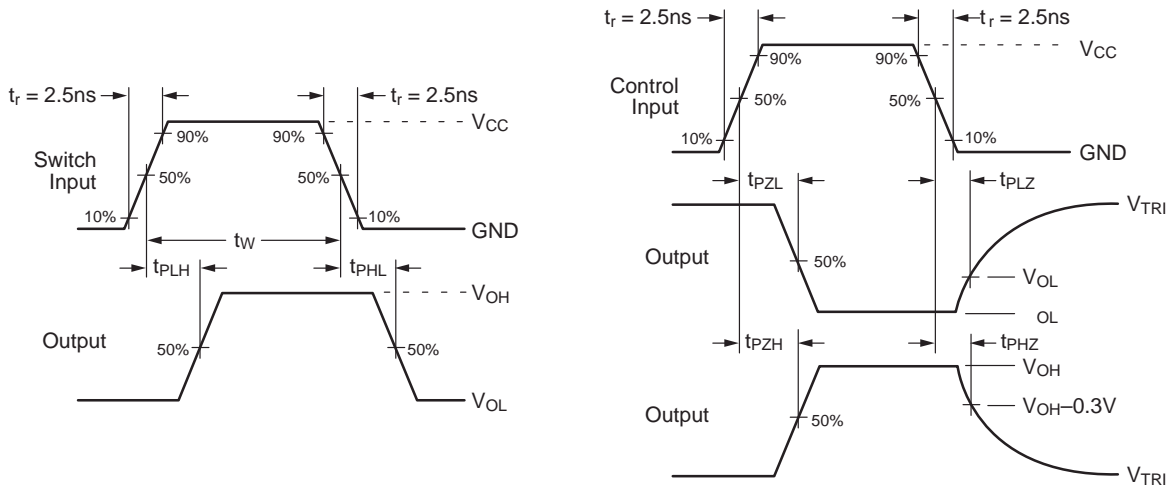


Figure 6. AC Waveforms

AC Loading and Waveforms (continued)

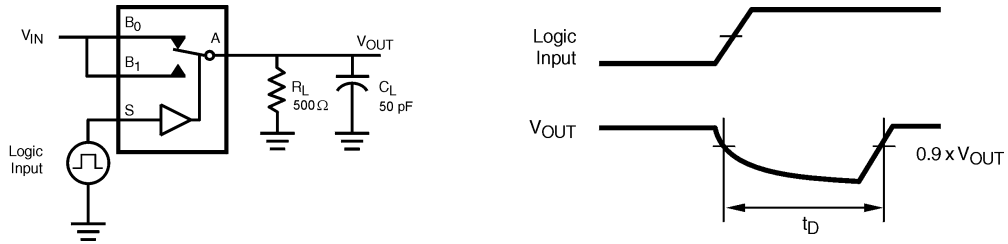


Figure 7. Break-Before-Make Interval Timing

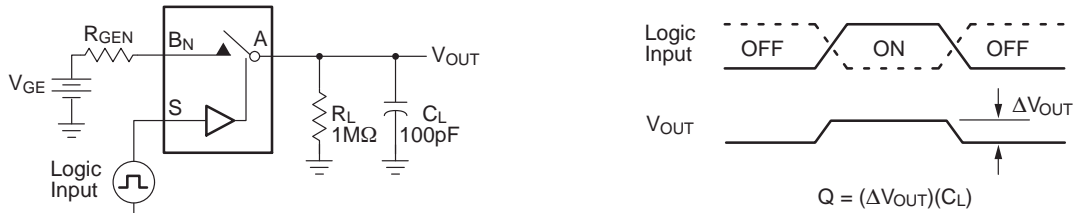


Figure 8. Charge Injection Test

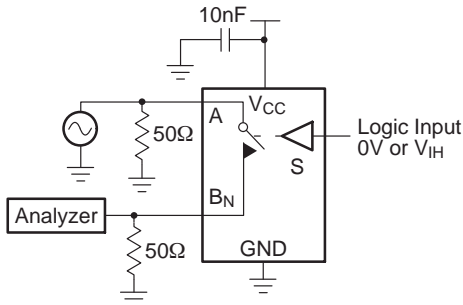


Figure 9. Off Isolation

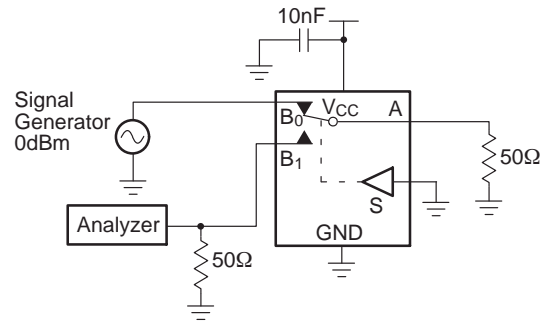


Figure 10. Crosstalk

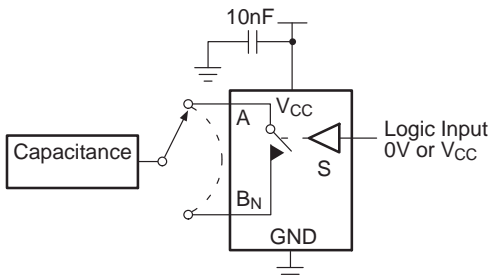


Figure 11. Channel Off Capacitance

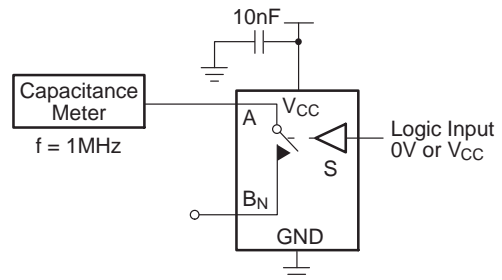


Figure 12. Channel On Capacitance

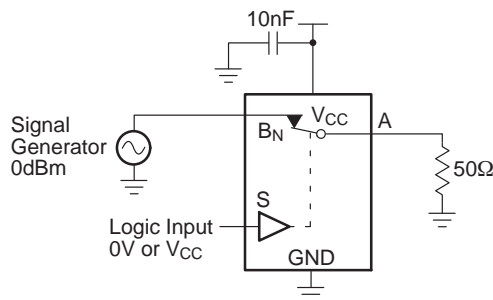


Figure 13. Bandwidth

# MECHANICAL CASE OUTLINE

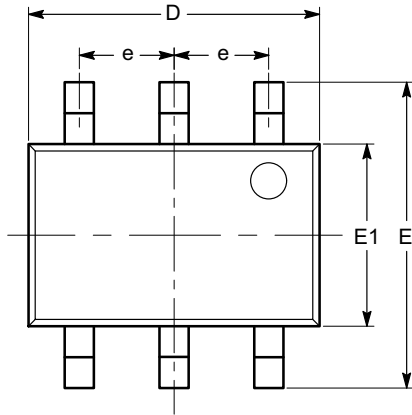
## PACKAGE DIMENSIONS

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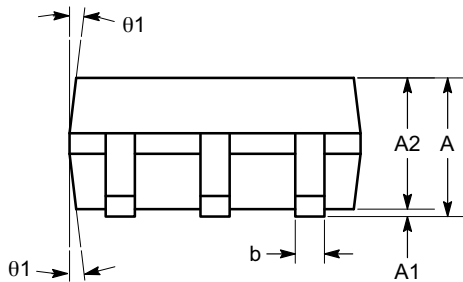
SC-88 (SC-70 6 Lead), 1.25x2  
CASE 419AD-01  
ISSUE A

DATE 07 JUL 2010

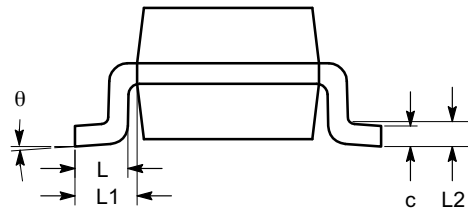


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
$\theta$	0°		8°
$\theta_1$	4°		10°



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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<b>DESCRIPTION:</b>	<b>SC-88 (SC-70 6 LEAD), 1.25X2</b>	<b>PAGE 1 OF 1</b>

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