CHANGE NOTIFICATION

Analog Devices, Inc.
1630 McCarthy Blvd., Milpitas CA
(408) 432-1900

June 15, 2017

Dear Sir/Madam: PCN# 061517

Subject: **Notification of Change to LTC4359 Die and Datasheet**

Please be advised that Analog Devices, Inc. Milpitas, California has made changes to the LTC4359 device to facilitate improvement in manufacturing yield.

Changes were made to the SHDN# pin current to improve its yield. The SHDN# pin internal pull-up current source was increased to better meet the $I_{SHDN\#}$ specification over temperature and manufacturing variation. This change slightly increases the OUT current (I_{OUT} in reverse bias condition) as shown on the attached datasheet mark-up. In addition, a metal layer was added to improve the interconnect.

The change was qualified by performing characterization over the full operating temperature range and by successfully passing High Temperature Operating Life, High Temp Storage Life, HAST, Autoclave (PCT), Thermal Shock Testing and Temperature Cycle. Product built using the new die and tested to the updated specification will be shipped with a datecode of approximately 1730.

Analog Devices will accept requests for revised samples within 30 days of the date of this notification. If we don't hear back from your company within this 30 day period, we will consider acceptance of this Change Notice by August 15, 2017.

Should you have any further questions, please feel free to contact your local Analog Devices Inc. sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail JASON.HU@ANALOG.COM.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, IN = 12V, SOURCE = IN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Supply Range		●	4		80	V
I_{IN}	IN Current	IN = 12V	●		150	200	µA
		IN = OUT = 12V, $\overline{SHDN}$ = 0V	●		9	20	µA
		IN = OUT = 24V, $\overline{SHDN}$ = 0V	●		15	30	µA
		IN = –40V	●	0	–15	–40	µA
I_{OUT}	OUT Current	IN = 12V, In Regulation	●	3	5	7.5	µA
		IN = 12V, ΔV_{SD} = –1V	●		120	~~200~~ 220	µA
		IN = OUT = 12V, $\overline{SHDN}$ = 0V	●		0.8	3	µA
		IN = OUT = 24V, $\overline{SHDN}$ = 0V	●		0.8	3	µA
		OUT = 12V, IN = $\overline{SHDN}$ = 0V	●		6	12	µA
I_{SOURCE}	SOURCE Current	IN = 12V, ΔV_{SD} = –1V	●		150	200	µA
		IN = SOURCE = 12V, $\overline{SHDN}$ = 0V	●	1	4	15	µA
		SOURCE = –40V	●	–0.4	–0.8	–1.5	mA
ΔV_{GATE}	Gate Drive (GATE–SOURCE)	IN = 4V, I_{GATE} = 0, –1µA	●	4.5	5.5	15	V
		IN = 8V to 80V; I_{GATE} = 0, –1µA	●	10	12	15	V
ΔV_{SD}	Source-Drain Regulation Voltage (IN –OUT)	ΔV_{GATE} = 2.5V	●	20	30	45	mV
$I_{GATE(UP)}$	Gate Pull-Up Current	GATE = IN, ΔV_{SD} = 0.1V	●	–6	–10	–14	µA
$I_{GATE(DOWN)}$	Gate Pull-Down Current	Fault Condition, ΔV_{GATE} = 5V, ΔV_{SD} = –1V	●	70	130	180	mA
		Shutdown Mode, ΔV_{GATE} = 5V, ΔV_{SD} = 0.7V	●	0.6			mA
t_{OFF}	Gate Turn-Off Delay Time	ΔV_{SD} = 0.1V to –1V, ΔV_{GATE} < 2V, C_{GATE} = 0pF	●		0.3	0.5	µs
t_{ON}	Gate Turn-On Delay Time	IN = 12V, SOURCE = OUT = 0V, $\overline{SHDN}$ = 0V to 2V ΔV_{GATE} > 4.5V, C_{GATE} = 0pF			200		µs
$V_{SHDN(TH)}$	$\overline{SHDN}$ Pin Input Threshold	IN = 4V to 80V	●	0.6	1.2	2	V
$V_{SHDN(FLT)}$	$\overline{SHDN}$ Pin Float Voltage	IN = 4V to 80V	●	0.6	1.75	2.5	V
I_{SHDN}	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ = 0.5V, LTC4359I, LTC4359C	●	–1	~~–2.6~~ –3	–5	µA
		$\overline{SHDN}$ = 0.5V, LTC4359H	●	–0.5	~~–2.6~~ –3	–5	µA
		$\overline{SHDN}$ = –40V	●	–0.4	–0.8	–1.5	mA
		Maximum Allowable Leakage, V_{IN} = 4V			100		nA
$V_{SOURCE(TH)}$	Reverse SOURCE Threshold for GATE Off	GATE = 0V, $I_{GATE(DOWN)}$ = 1mA	●	–0.9	–1.8	–2.7	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into pins are positive; all voltages are referenced to V_{SS} unless otherwise specified.

Note 3. An internal clamp limits the OUT pin to a minimum of 100V above V_{SS}. Driving this pin with more current than 1mA may damage the device.

Note 4. An internal clamp limits the GATE pin to a minimum of 10V above IN or 100V above V_{SS}. Driving this pin to voltages beyond the clamp may damage the device.