



**Synchronous Buck
 Multiphase Optimized BGA Power Block**
 Integrated Power Semiconductors, Drivers & Passives

Features:

- 20A continuous output current with no derating up to $T_{PCB} = 90^{\circ}\text{C}$
- Very small 11mm x 11mm x 3mm profile
- Internal features minimize layout sensitivity *
- Optimized for very low power losses
- 3.3 to 12V input voltage

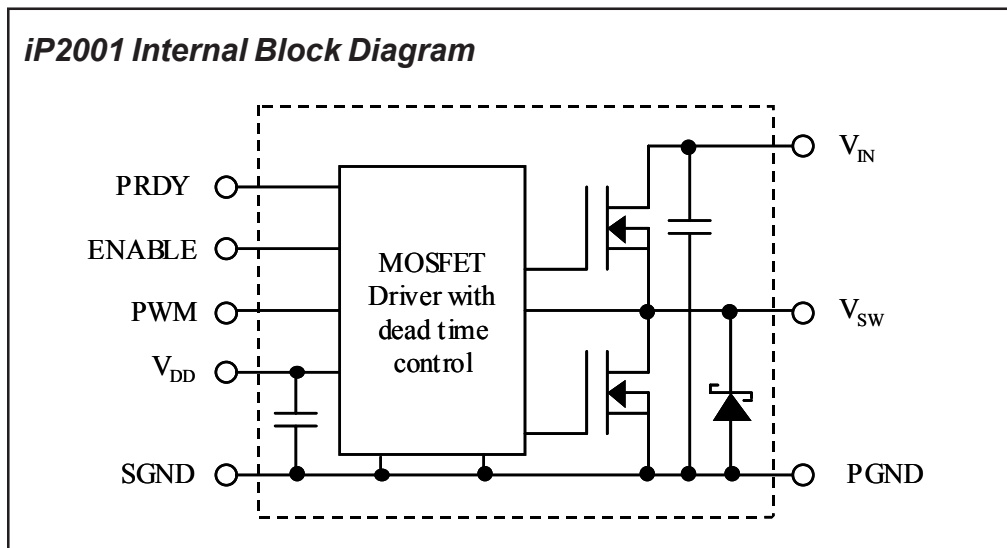


iP2001 Power Block

Description

The iP2001 is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 11mm x 11mm x 3mm BGA power block. The only additional components required for a complete multiphase converter are a PWM IC, the external inductors, and the input and output capacitors.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.



* All of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR Block. There are no concerns about double pulsing, unwanted shutdown, or other malfunctions which often occur in switching power supplies. The iPOWIR Block will function normally without any additional input power supply bypass capacitors. However, for reliable long term operation it is recommended that the adequate amount of input decoupling is provided on the V_{IN} pin. No additional bypassing is required on the V_{DD} pin.

iP2001

All specifications @ 25°C (unless otherwise specified)

Absolute Maximum Ratings :

| Parameter | Min | Typ | Max | Units | Conditions |
|---------------------|------|-----|----------------|-------|--------------------|
| V_{IN} to PGND | - | - | 16 | V | |
| V_{DD} to SGND | - | - | 6.0 | V | |
| PWM to SGND | -0.3 | - | $V_{DD} + 0.3$ | V | not to exceed 6.0V |
| Enable to SGND | -0.3 | - | $V_{DD} + 0.3$ | V | not to exceed 6.0V |
| Output RMS Current | - | - | 20 | A | |
| Storage Temperature | -40 | - | 125 | °C | |

Recommended Operating Conditions :

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|----------------------|-----------|-----|-----|------|-------|-----------------|
| Supply Voltage | V_{DD} | 4.6 | 5.0 | 5.5 | V | |
| Input Voltage Range | V_{IN} | 3.0 | - | 12.6 | V | |
| Output Voltage Range | V_{OUT} | 0.9 | - | 3.3 | V | see Figs. 2 & 4 |
| Output Current Range | I_{OUT} | - | - | 20 | A | see Fig. 2 |
| Operating Frequency | fsw | 150 | - | 1000 | kHz | see Figs. 2 & 5 |
| Operating Duty Cycle | D | - | - | 85 | % | |

Electrical Specifications @ $V_{DD} = 5V$ (unless otherwise specified) :

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|--|----------------|-----|-----|-----|-------|---|
| Block Power Loss ① | P_{BLK} | - | 3.1 | 3.8 | W | $V_{IN} = 12V, V_{OUT} = 1.6V,$ $I_{OUT} = 20A, f_{sw} = 500kHz$ |
| Turn On Delay ② | $t_{d(on)}$ | - | 63 | - | ns | |
| Turn Off Delay ② | $t_{d(off)}$ | - | 26 | - | | |
| V_{IN} Quiescent Current | I_{Q-VIN} | - | - | 1.0 | mA | Enable = 0V, $V_{IN} = 12V$ |
| V_{DD} Quiescent Current | I_{Q-VDD} | - | - | 10 | μA | Enable = 0V, $V_{DD} = 5V$ |
| Under Voltage Lockout Start Threshold | V_{START} | 4.2 | 4.4 | 4.5 | V | |
| Hysteresis | $V_{Hys-UVLO}$ | - | .05 | - | | |
| Enable Input Voltage High | V_{IH} | 2.0 | - | - | V | |
| Input Voltage Low | V_{IL} | - | - | 0.8 | | |
| Power Ready Logic Level High | V_{OH} | 4.5 | 4.6 | - | V | $V_{DD} = 4.6V, I_{Load} = 10mA$ |
| Logic Level Low | V_{OL} | - | 0.1 | 0.2 | | $V_{DD} < UVLO \text{ Threshold}, I_{Load} = 1mA$ |
| PWM nput Logic Level High | V_{OH} | 2.0 | - | - | V | |
| Logic Level Low | V_{OL} | - | - | 0.8 | | |

① Measurement were made using four 10uF (TDK C3225X7R1C106M or equiv.) capacitors across the input (see Fig. 8).

② Not associated with the rise and fall times. Does not affect Power Loss (see Fig. 9).

Pin Description Table

| Pin Name | Ball Designator | Pin Function |
|-----------------|---|--|
| V _{DD} | A1 – A3, B1 – B3 | Supply voltage for the internal circuitry. |
| V _{IN} | A5 – A12, B5 – B12, C5 - C10 | Input voltage for the DC-DC converter. |
| PGND | C11, C12, D11, D12, E11, E12, F6, F7, F12, G6, G7, G12, H6, H7, H12, J6, J7, J12, K5 – K7, K12, L5, L6, L12, M5 – M7, M12 | Power Ground - connection to the ground of bulk and filter capacitors. |
| V _{SW} | D5 – D10, E5 – E10, F8 – F11, G8 – G11, H8 – H11, J8 – J11, K8 – K11, L8 – L11, M8 – M11 | Switching Node - connection to the output inductor. |
| SGND | C1 – C3, D1 –D3, E1 –E3 | Signal Ground. |
| ENABLE | F1 | When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the PRDY pin is forced low, the Control and Synchronous switches are turned off, and the supply current is less than 10μA. |
| PRDY | K1 | Power Ready - This pin indicates the status of ENABLE or V _{DD} . This output will be driven low when ENABLE is logic low or when V _{DD} is less than 4.4V (typ.). When ENABLE is logic high and V _{DD} is greater than 4.4V (typ.), this output is driven high. This output has a 10mA source and 1mA sink capability. |
| PWM | H1 | TTL-level input signal to MOSFET drivers. |
| NC | B4, C4, D4, E4, F2 – F4, G2 – G4, H2 – H4, J1, J2 – J4, K3, L1, L2, M1 – M4 | This pin is not for electrical connection. It should be attached only to dead copper. |

iP2001

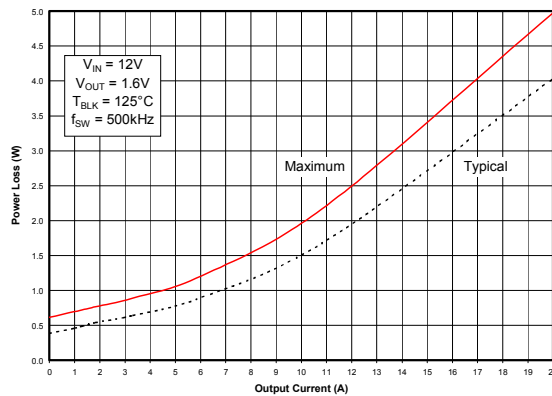


Fig 1. Power Loss vs. Current

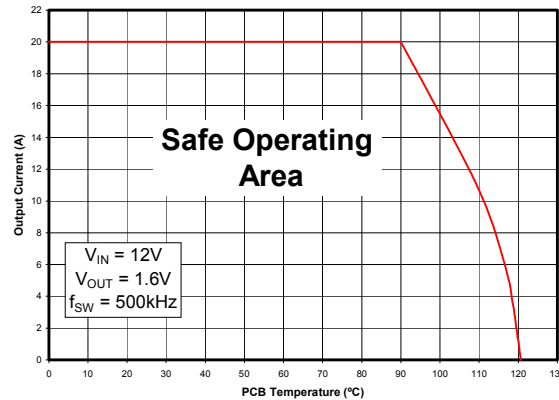


Fig 2. Safe Operating Area (SOA) vs. T_{PCB} *
(*see AN-1030 for details)

Adjusting the Power Loss and SOA curves for different operating conditions

To make adjustments to the power loss curves in Fig. 1, multiply the normalized value obtained from the curves in Figs. 3, 4, 5 or 6 by the value indicated on the power loss curve in Fig. 1. If multiple adjustments are required, multiply all of the normalized values together, then multiply that product by the value indicated on the power loss curve in Fig. 1. The resulting product is the final power loss based on all factors.

To make adjustments to the SOA curve in Fig. 2, determine the maximum allowed PCB temperature in Fig. 2 at the required operating current. Then, add the correction temperature from the normalized curves in Figs. 3, 4, 5 or 6 to find the final maximum allowable PCB temperature. When multiple adjustments are required, add all of the temperatures together, then add the sum to the PCB temperature indicated on the SOA graph to determine the final maximum allowable PCB temperature based on all factors.

Operating Conditions for the examples below:

Output Current = 20A Input Voltage = 7V
Output Voltage = 2.5V Sw Freq= 750kHz

Adjusting for Maximum Power Loss:

- (Fig. 1) Maximum power loss = 5W
- (Fig. 3) Normalized power loss for input voltage ≈ 0.925
- (Fig. 4) Normalized power loss for output voltage ≈ 1.1
- (Fig. 5) Normalized power loss for frequency ≈ 1.225

$$\text{Adjusted Power Loss} = 5W \times 1.1 \times 0.925 \times 1.225 \approx 6.23W$$

Adjusting for SOA Temperature:

- (Fig. 2) SOA PCB Temperature = 90°C
- (Fig. 3) Normalized SOA PCB Temperature for input voltage $\approx 2.6^\circ\text{C}$
- (Fig. 4) Normalized SOA PCB Temperature for output voltage $\approx -3.5^\circ\text{C}$
- (Fig. 5) Normalized SOA PCB Temperature for frequency $\approx -7.5^\circ\text{C}$

$$\text{Adjusted SOA PCB Temperature} = 90^\circ\text{C} - 3.5^\circ\text{C} + 2.6^\circ\text{C} - 7.5^\circ\text{C} \approx 81.6^\circ\text{C}$$

Typical Performance Curves

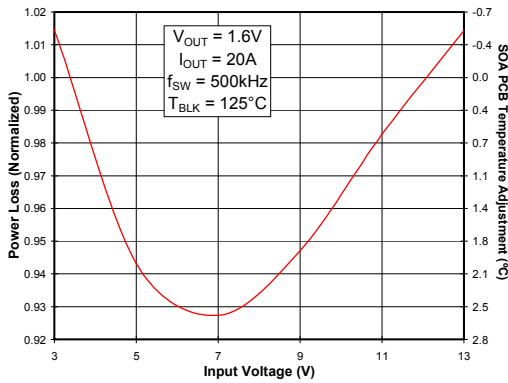


Fig 3. Normalized Power Loss vs. V_{IN}

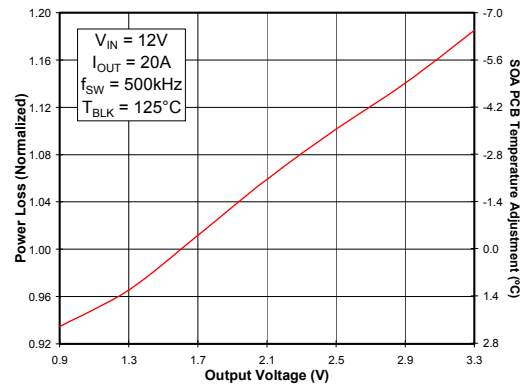


Fig 4. Normalized Power Loss vs. V_{OUT}

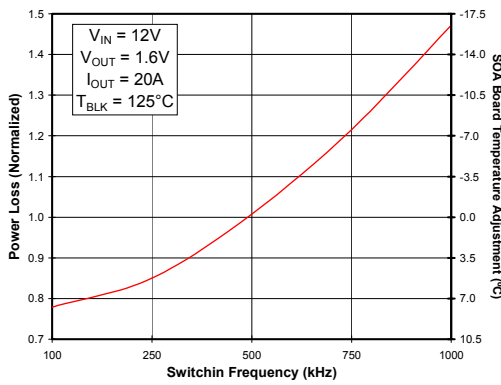


Fig 5. Normalized Power Loss vs. Frequency

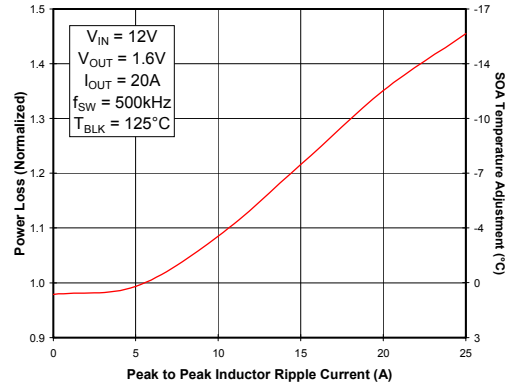


Fig 6. Normalized Power Loss vs. Ripple Current

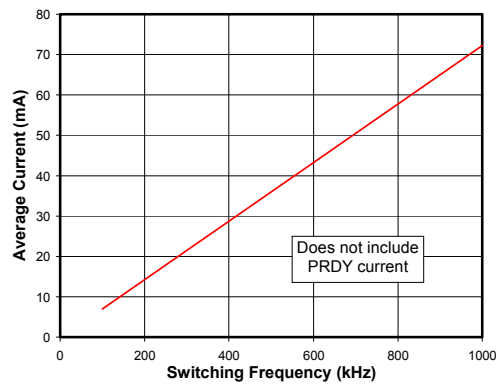
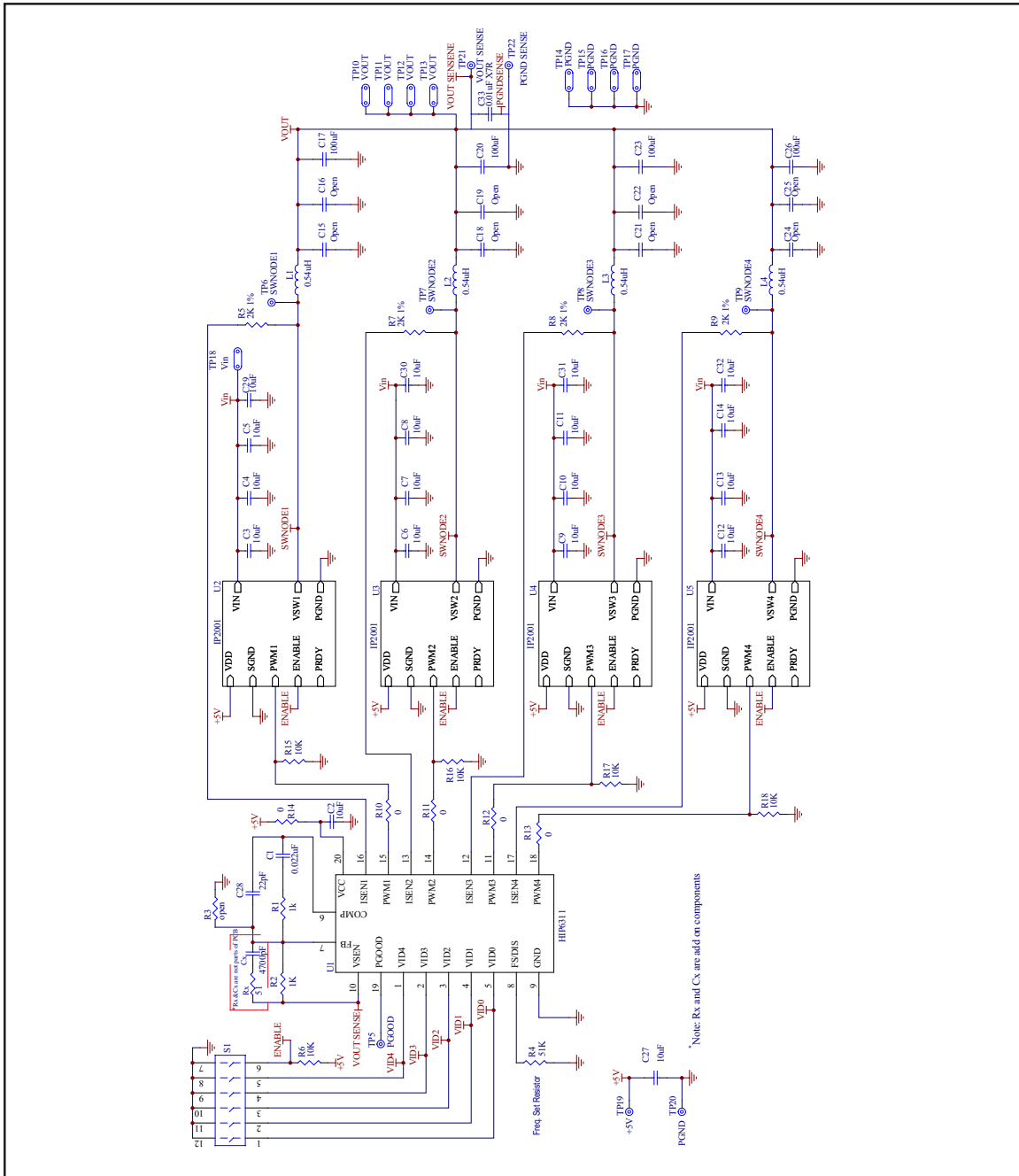


Fig 7. I_{DD} vs. Frequency



4-Phase Reference Design Schematic

| Designator | Value 1 | Value 2 | Type | Tolerance | Package | Mfr. | Mfr. Part No. |
|--|---------|------------|----------------|-----------|---------------|----------------|----------------|
| C1 | 0.022uF | 50V | X7R | 10% | 0805 | TDK | C2012X7R1H223K |
| C2 - C14, C27, C29 - C32 | 10.0uF | 16V | X5R | 10% | 1210 | TDK | C3225X5R1C106K |
| C15, C16, C18, C19, C21, C22, C24, C25, D1 - D4, R3, R19 | - | - | - | - | - | - | - |
| C17, C20, C23, C26 | 100uF | 6.3V | X5R | 10% | 2220 | TDK | C5750X5R0J107K |
| C28 | 22.0pF | 50V | COG | 5% | 0805 | TDK | C2012COG1H220J |
| C33 | 0.010uF | 50V | X7R | 10% | 0805 | TDK | C2012X7R1H103K |
| Cx | 4700pF | 50V | X7R | 10% | 0603 | TDK | C1608X7R1H472K |
| L1 - L4 | 0.54uH | 27A | Ferrite | 20% | SMT | Panasonic | ETQP6F0R6BFA |
| R1, R2 | 1K | 1/8W | Thick film | 5% | 0805 | ROHM | MCR10EZJH102 |
| R10 - R14 | 0 | 1/8W | Thick film | <50m | 0805 | ROHM | MCR10EZJH000 |
| R6, R15 - R18 | 10K | 1/8W | Thick film | 5% | 0805 | ROHM | MCR10EZJH103 |
| R4 | 51K | 1/8W | Thick film | 5% | 0805 | ROHM | MCR10EZJH513 |
| R5, R7, R8, R9 | 2K | 1/8W | Thick film | 5% | 0805 | ROHM | MCR10EZJH202 |
| Rx | 51 | 1/10W | Thick film | 5% | 0603 | KOA | RM73B1J510J |
| S1 | SPST | 6 position | Switch | - | SMT | C&K Components | SD06H0SK |
| ST1 - ST4 | 4-40 | - | - | - | - | Keystone | 8412 |
| U1 | - | - | PWM controller | 0 - 70°C | SOIC20 | Intersil | HIP6311CB |
| U2 - U5 | - | - | DC-DC | - | 11 x 11 x 3mm | IR | IP2001 |

4-Phase Reference Design Bill of Materials

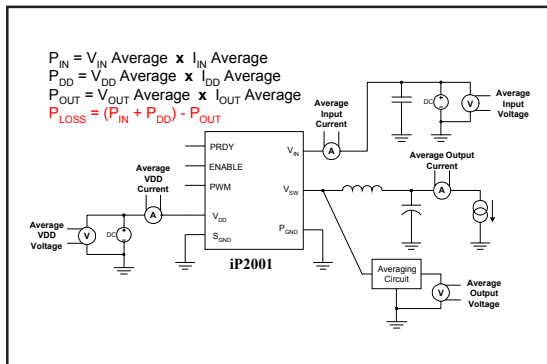


Fig 8. Power Loss Test Circuit

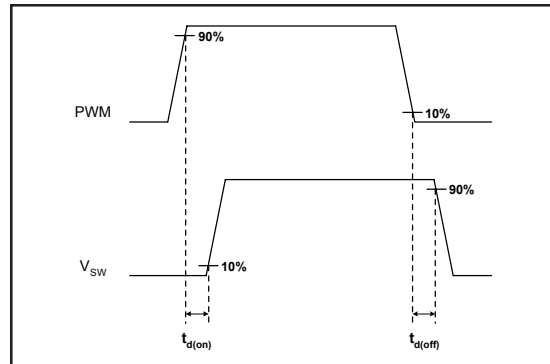
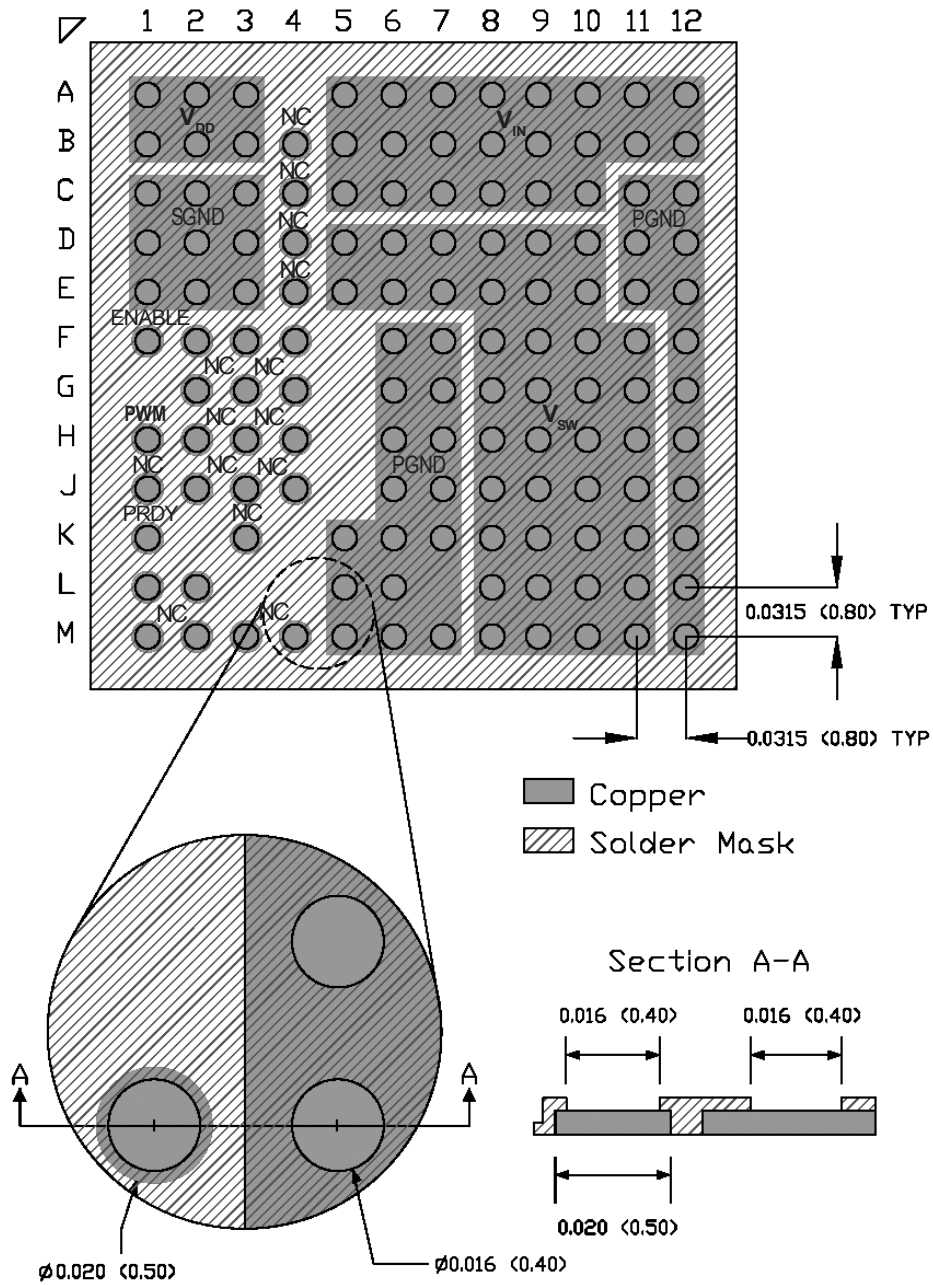
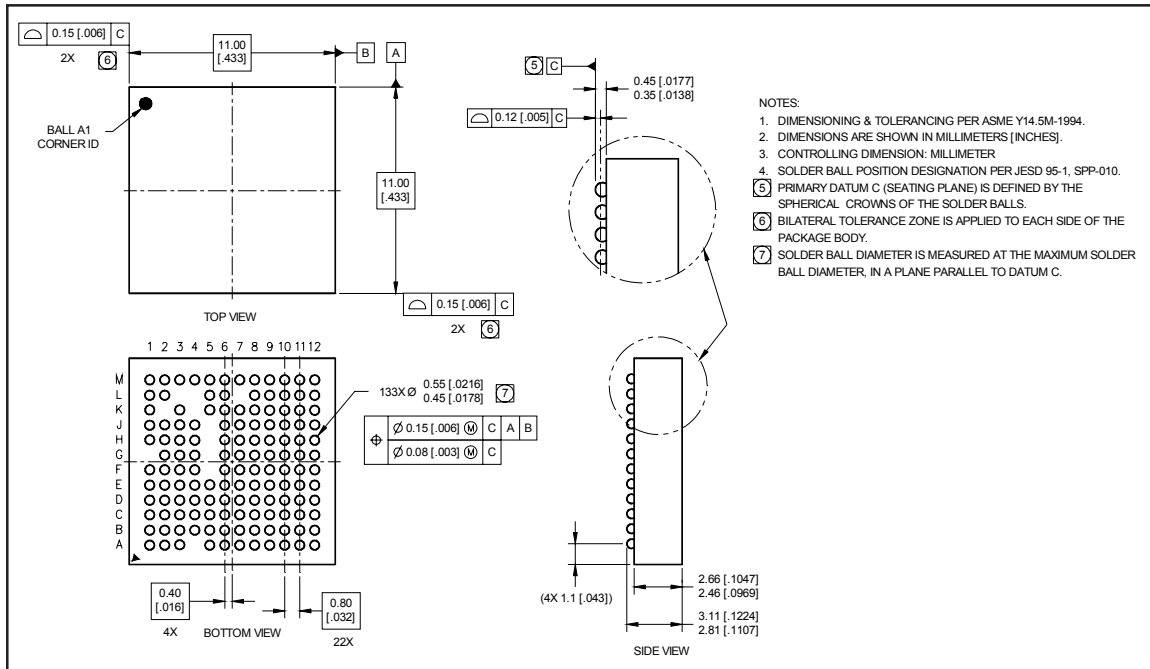


Fig 9. Timing Diagram



Recommended PCB Footprint (Top View)



Mechanical Drawing

Refer to the following application notes for detailed guidelines and suggestions when implementing iPOWIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages

This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

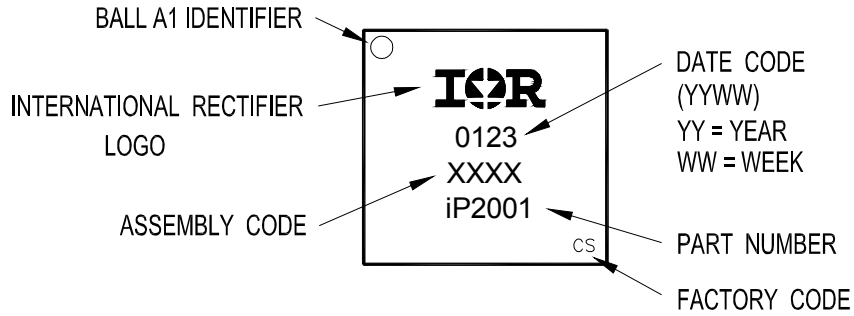
AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design

This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

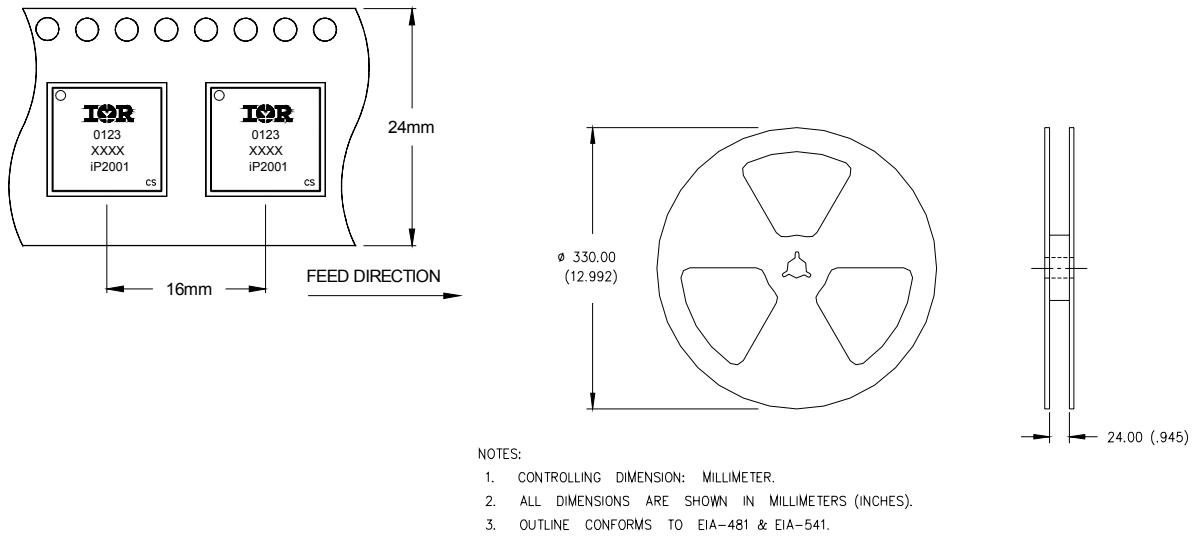
AN-1030: Applying iPOWIR Products in Your Thermal Environment

This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

iP2001



Part Marking



Tape & Reel Information

*Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.*

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.8/01